Infrared Data Association
Serial Infrared
Physical Layer Specification

Version 1.4

May 30th, 2001

Authors

Many people contributed to this physical layer document, primarily from Hewlett-Packard, IBM, Vishay and Sharp.
Editor of Version 1.4:
Wee-Sin Tan of Agilent Technologies, (65) 215-7200 (65) 278-0791, wee-sin_tan@agilent.com
Editor of the VFIR physical layer
John Petrilla of Agilent Technologies, San Jose, CA, USA
Walter Hirt of IBM Research Division, Zurich Research Laboratory, Ruschlikon, Switzerland
Youichi Yuuki of Sharp Corporation, Optoelectronics Device Division, Electronic Component Group, Nara, Japan
Editor of version 1.3 and author of appendices (Test Methods and Examples):
John Petrilla of HP, (408)435-6608, (408)435-6286 (fax), john_petrilla@hp.com
Author of low power option extension to 0.576 Mbit/s, 1.152 Mbit/s and 4.0 Mbit/s data rates:
Raymond Quek of HP, (65) 2798871, (65) 2780791 (fax), raymond_quek@hp.com
The primary author and editor of versions 1.0 through 1.2:
Joe Tajnai of HP, (408)435-6331, (408)435-6286 (fax), joe_tajnai@hp.com.

Contributor

Dr. Jorg Angerstein of Vishay Semiconductor GmbH, Heilbronn, Germany

Document Status

Version 1.0 was approved at the IrDA meeting on April 27, 1994.
Version 1.1 was approved at the IrDA meeting on October 17, 1995.
Version 1.2 was approved at the IrDA meeting on October 16, 1997.
Minor edits were done after the meeting.
Version 1.3 was approved at the IrDA meeting on October 15, 1998.
Minor edits were made after the meeting

NOTE: Version 1.4 Obsoletes and Replaces Version 1.3

Current Changes

(Changes from Version 1.3, approved on Oct 15, 1998)
Merging of the errata (Jan 8 1999) which contains the;
Extension of Physical layer specifications for 16.0 Mbit/s data rates,
proposal for a new modulation code for 16.0 Mbit/s rate, and
addition of new signaling rate and encoding and decoding examples for 16.0 Mbit/s rate.
Inclusion of the Amendment 2 calculations to the eye safety standards

Prior Changes

(Changes from Version 1.2, Errata approved Oct. 15, '98, Document edits completed Nov. 20 '98)
Low power option extended to 0.576 Mbit/s, 1.152 Mbit/s and 4.0 Mbit/s data rates.
Recommendation added of higher EMI test ambient for operation with or near mobile phone or pager.
Appendix B.4. revised to include examples for standard, low power and mixed operation at 1.152 Mbit/s and 4.0 Mbit/s and tables reformatted for consistency. Noise calculations revised for better match with model.
Various typographical errors corrected.

(Changes from Version 1.1)
Low power option added.
Information regarding eye safety standards and compliance added.
Examples added for low power option and low power option/standard combination.
All examples, except 1.152Mbit/s, recalculated and reformatted for consistency.

INFRARED DATA ASSOCIATION (IrDA) - NOTICE TO THE TRADE -

SUMMARY:
Following is the notice of conditions and understandings upon which this document is made available to members and non-members of the Infrared Data Association.

- Availability of Publications, Updates and Notices
- Full Copyright Claims Must be Honored
- Controlled Distribution Privileges for IrDA Members Only
- Trademarks of IrDA - Prohibitions and Authorized Use
- No Representation of Third Party Rights
- Limitation of Liability
- Disclaimer of Warranty
- Product Testing for IrDA Specification Conformance

IrDA PUBLICATIONS and UPDATES:

IrDA publications, including notifications, updates, and revisions, are accessed electronically by IrDA members in good standing during the course of each year as a benefit of annual IrDA membership. Electronic copies are available to the public on the IrDA web site located at irda.org. Requests for publications, membership applications or more information should be addressed to: Infrared Data Association, P.O. Box 3883, Walnut Creek, California, U.S.A. 94598; or e-mail address: info@irda.org; or by calling (925) 943-6546 or faxing requests to (925) 943-5600.

COPYRIGHT:

1. Prohibitions: IrDA claims copyright in all IrDA publications. Any unauthorized reproduction, distribution, display or modification, in whole or in part, is strictly prohibited.

2. Authorized Use: Any authorized use of IrDA publications (in whole or in part) is under NONEXCLUSIVE USE LICENSE ONLY. No rights to sublicense, assign or transfer the license are granted and any attempt to do so is void.

TRADEMARKS:

1. Prohibitions: IrDA claims exclusive rights in its trade names, trademarks, service marks, collective membership marks and feature trademark marks (hereinafter collectively "trademarks"), including but not limited to the following trademarks: INFRARED DATA ASSOCIATION (wordmark alone and with IR logo), IrDA (acronym mark alone and with IR logo), IR logo and MEMBER IrDA (wordmark alone and with IR logo). Any unauthorized use of IrDA trademarks is strictly prohibited.

2. Authorized Use: Any authorized use of an IrDA collective membership mark or feature trademark is by NONEXCLUSIVE USE LICENSE ONLY. No rights to sublicense, assign or transfer the license are granted and any attempt to do so is void.

NO REPRESENTATION of THIRD PARTY RIGHTS:

IrDA makes no representation or warranty whatsoever with regard to IrDA member or third party ownership, licensing or infringement/non-infringement of intellectual property rights. Each recipient of IrDA publications, whether or not an IrDA member, should seek the independent advice of legal counsel with regard to any possible violation of third party rights arising out of the use, attempted use, reproduction, distribution or public display of IrDA publications.

IrDA assumes no obligation or responsibility whatsoever to advise its members or non-members who receive or are about to receive IrDA publications of the chance of infringement or violation of any right of an IrDA member or third party arising out of the use, attempted use, reproduction, distribution or display of IrDA publications.

LIMITATION of LIABILITY:

BY ANY ACTUAL OR ATTEMPTED USE, REPRODUCTION, DISTRIBUTION OR PUBLIC DISPLAY OF ANY IrDA PUBLICATION, ANY PARTICIPANT IN SUCH REAL OR ATTEMPTED ACTS, WHETHER OR NOT A MEMBER OF IrDA, AGREES TO ASSUME ANY AND ALL RISK ASSOCIATED WITH SUCH ACTS, INCLUDING BUT NOT LIMITED TO LOST PROFITS, LOST SAVINGS, OR OTHER CONSEQUENTIAL, SPECIAL, INCIDENTAL OR PUNITIVE DAMAGES. IrDA SHALL HAVE NO LIABILITY WHATSOEVER FOR SUCH ACTS NOR FOR THE CONTENT, ACCURACY OR LEVEL OF ISSUE OF AN IrDA PUBLICATION.

DISCLAIMER of WARRANTY:

All IrDA publications are provided "AS IS" and without warranty of any kind. IrDA (and each of its members, wholly and collectively, hereinafter "IrDA") EXPRESSLY DISCLAIM ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE AND WARRANTY OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.
IrDA DOES NOT WARRANT THAT ITS PUBLICATIONS WILL MEET YOUR REQUIREMENTS OR THAT ANY USE OF A PUBLICATION WILL BE UN-INTERRUPTED OR ERROR FREE, OR THAT DEFECTS WILL BE CORRECTED. FURTHERMORE, IrDA DOES NOT WARRANT OR MAKE ANY REPRESENTATIONS REGARDING USE OR THE RESULTS OR THE USE OF IrDA PUBLICATIONS IN TERMS OF THEIR CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. NO ORAL OR WRITTEN PUBLICATION OR ADVICE OF A REPRESENTATIVE (OR MEMBER) OF IrDA SHALL CREATE A WARRANTY OR IN ANY WAY INCREASE THE SCOPE OF THIS WARRANTY.

LIMITED MEDIA WARRANTY:

IrDA warrants ONLY the media upon which any publication is recorded to be free from defects in materials and workmanship under normal use for a period of ninety (90) days from the date of distribution as evidenced by the distribution records of IrDA. IrDA's entire liability and recipient's exclusive remedy will be replacement of the media not meeting this limited warranty and which is returned to IrDA. IrDA shall have no responsibility to replace media damaged by accident, abuse or misapplication. ANY IMPLIED WARRANTIES ON THE MEDIA, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO NINETY (90) DAYS FROM THE DATE OF DELIVERY. THIS WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, AND YOU MAY ALSO HAVE OTHER RIGHTS WHICH VARY FROM PLACE TO PLACE.

COMPLIANCE and GENERAL:

Membership in IrDA or use of IrDA publications does NOT constitute IrDA compliance. It is the sole responsibility of each manufacturer, whether or not an IrDA member, to obtain product compliance in accordance with IrDA Specifications.

All rights, prohibitions of right, agreements and terms and conditions regarding use of IrDA publications and IrDA rules for compliance of products are governed by the laws and regulations of the United States. However, each manufacturer is solely responsible for compliance with the import/export laws of the countries in which they conduct business. The information contained in this document is provided as is and is subject to change without notice.

Table of Contents

Figures

Tables

1. Introduction

1.1. Scope

This physical specification is intended to facilitate the point-to-point communication between electronic devices (e.g., computers and peripherals) using directed half duplex serial infrared communications links through free space. This document specifies the optical media interfaces for Serial Infrared (SIR) data transmission up to and including 115.2 kbit/s, 0.576 Mbit/s, 1.152 Mbit/s, 4.0 Mbit/s and 16 Mbit/s. It contains specifications for the Active Output Interface and the Active Input Interface, and for the overall link. It also contains Appendices covering test methods and implementation examples.

Over the past several years several optical link specifications have been developed. This activity has established the advantages of optical interface specifications to define optical link parameters needed to support the defined link performance. Optical interface specifications are independent of technology, apply over the life of the link and are readily testable for conformance. The IrDA serial infrared link specification supports low cost optoelectronic technology and is designed to support a link between two nodes from 0 to at least 1 meter apart (20 cm for low power parts: please see Section 4.1) as shown in Figure 1 (the two ports need not be perfectly aligned).

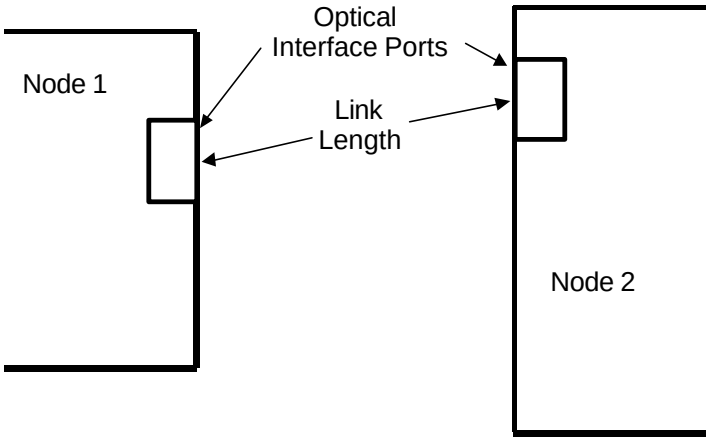


Figure 1. Schematic View of the Optical Interface Port Geometry

1.2. References

The following standards either contain provisions that, through reference in this text, constitute provisions of this proposed standard, or provide background information. At the time of publication of this document, the editions and dates of the referenced documents indicated were valid. However, all standards are subject to revision, and parties to agreements based on this proposed standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

IrDA (Infrared Data Association) Serial Infrared Link Access Protocol (IrLAP), Version 1.1, June 16, 1996.

IrDA (Infrared Data Association) Serial Infrared Link Management Protocol, IrLMP), Version 1.1, January 23, 1996.

IrDA (Infrared Data Association) Serial Infrared Physical Layer Measurement Guidelines, Version 1.0, January 16, 1998.

IrDA (Infrared Data Association) IrMC Specification, Version 1.0.1, January 10, 1998.

IEC Standard Publication 61000-4-3: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 3: Radiated Electromagnetic Field Measurements.

IEC 60825-1:(1993) Safety of laser products-Part 1: Equipment classification, requirements and user's guide, as amended (reported at TC 76 Meeting, Frankfurt, Germany, October 31, 1997) and Amendment 2 to IEC 60825-1 (dtd 17 Oct 2000).

CENELEC EN 60825-1/A11 (October 1996) (amendment to CENELEC version of IEC 60825-1:(1993)

1.3. Abbreviations & Acronyms

4PPM = Four Pulse Position Modulation
A = Address field
Base = Number of pulse positions (chips) in each data symbol
BER = Bit Error Ratio
Bwr = Receiver Bandwidth
Bwrl = Receiver Band Lower Cutoff Frequency
Bwru = Receiver Band Upper Cutoff Frequency
C = Control field
CCITT = International Consultative Committee for Telephone and Telegraph; now ITU-T (CCITT is obsolete term). CCITT used in CRC codes.
CENELEC = European Committee for Electrotechnical Standardization
Chip = One time slice in a PPM symbol
cm = centimeter(s)
CRC32 = 32 bit IEEE 802.x Cyclic Redundancy Check Field
Ct = Duration of one chip
dB = decibel(s)
DBP = Data Bit Pair
DD = PPM encoded data symbol
Dt = Duration of one data symbol
EIA = Electronic Industries Association
FCS = Frame Check Sequence
FIR = Fast (Serial) Infrared (used to describe the data rates above 115.2 kbit/s up to 4 Mbit/s;obsolete term)
HDLC = High level Data Link Control
I = Information field
IEC = International Electrotechnical Commission
IR = Infrared
IRLAP = Infrared Link Access Protocol (document), also IrLAP
IRLMP = Infrared Link Management Protocol (document), also IrLMP
ITU-T = International Technical Union - Telecommunication (new name of old CCITT)
kBd = kilobaud
kbit/s = kilobits per second
kHz = kilohertz
LSB = Least Significant Bit
LP=Low Power Option
m = meter(s)
mA = milliampere(s)
Mbd = Megabaud
Mbit/s = Megabits per second
MHz = MegaHertz
mW = milliwatt(s)
ms = millisecond(s)
MSB = Most Significant Bit
nA = nanoampere(s)
ns = nanosecond(s)
pA = picoampere(s)
PA = Preamble

Payload Data = Real, unencoded data bytes transmitted in any packet
PLL = Phase Locked Loop
PPM = Pulse Position Modulation
RZ = Return-to-Zero
RZI = Return-to-Zero-Inverted
RLL = Run Length Limited (code)
SCC = Serial Communication Controller
SIP = Serial Infrared Interaction Pulse
SIR = Serial Infrared (used to describe infrared data transmission up to and including 115.2 kbit/s; obsolete term)
sr = Steradian
STA = Start Flag
STO = Stop Flag
Std = Standard Power Option
tf = Fall Time
tr = Rise Time
µA = microampere(s)
UART = Universal Asynchronous Receiver/Transmitter
Up = Peak Wavelength
µA = microampere(s)
µs = microsecond(s)
µW = microwatt(s)
V = volt(s)
VFIR = Very Fast (Serial) Infrared (used to describe infrared data transmission at 16.0 Mbit/s; obsolete term)

1.4. Definitions

1.4.1. Link Definitions

BER. Bit Error Ratio is the number of errors divided by the total number of bits. It is a probability, generally very small, and is often expressed as a negative power of 10 (e.g., 10^-8).

Angular Range is described by a spherical coordinate system (radial distance and angular coordinate relative to the z axis; the angular coordinate in the plane orthogonal to the z axis is usually ignored, and symmetry about the z axis is assumed) whose axis is normal to the emitting and receiving surface of the optical port and intersects the optical port at the center. The angular range is a cone whose apex is at the intersection of the optical axis and the optical interface plane.

Half-Angle (degrees) is the half angle of the cone whose apex is at the center of the optical port and whose axis is normal to the surface of the port (see Angular Range above). The half angle value is determined by the minimum angle from the normal to the surface where the Minimum Intensity In Angular Range is encountered.

Angular subtense is the angle (in degrees or radians) which an object, such as an emitter or detector or aperture covers at a specified distance (e.g., the Sun, viewed from the Earth, subtends and angle of approximately 0.5°).

1.4.2. Active Output Interface Definitions

Maximum Intensity In Angular Range, power per unit solid angle (milliwatts per steradian), is the maximum allowable source radiant intensity within the defined angular range (See Angular Range definition in Section 1.4.1.).

Minimum Intensity In Angular Range, power per unit solid angle (milliwatts or microwatts per steradian), is the minimum allowable source radiant intensity within the defined angular range (See Angular Range definition in Section 1.4.1.).

Rise Time Tr, 10-90%, and Fall Time Tf, 90-10% (microseconds or nanoseconds). These are the time intervals for the pulse to rise from 10% to 90% of the 100% value (not the overshoot value), and to fall from 90% to 10% of the 100% value.

Optical Over Shoot, % of Full (or 100%), is the peak optical signal level above the steady state maximum, less the steady state maximum, expressed as a % of the steady state maximum.

Signaling Rate, (kilobits per second or megabits per second). The rate at which information (data and protocol information) is sent or received.

Pulse Duration, % of bit period. This is the duration of the optical pulse, measured between 50% amplitude points (relative to the 100% value, not the overshoot value), divided by the duration of the bit or symbol period (depending on the modulation scheme), expressed as a percentage. This parameter is used in the duty factor conversion between average and peak power measurements.

Edge Jitter, %. For rates up to and including 115.2 kbit/s, this is the maximum deviation within a frame of an actual leading edge time from the expected value. The expected value is an integer number of bit duration (reciprocal of the signaling rate) after the reference or start pulse leading edge. The jitter is expressed as a percentage of the bit duration.

For 0.576 Mbit/s and 1.152 Mbit/s rates, the jitter is defined as one half of the worst case deviation in time delay between any 2 edges within 32 bit durations of one another, from the nearest integer multiple of the average bit duration. In other words, at 1.151 Mb/s (valid deviation from 1.152 Mb/s), if two pulses can be found in a transmitted frame whose edges are separated by 25.10 microseconds, this would be out of spec., since the nearest integer multiple of the bit duration is 25.195 microseconds, so the observed delay is more than twice 2.9% of a bit period (50.3 nanoseconds) different from the expected delay.

For 4.0 Mbit/s and 16.0 Mbit/s, both leading and trailing edges are considered. From an eye diagram (see measurements section-Appendix A), the edge jitter is the spread of the 50% leading and trailing times. The jitter is expressed as a percentage of the symbol duration.

Peak Wavelength (nanometers). Wavelength at which the optical output source intensity is a maximum.

1.4.3. Active Input Interface Definitions

Maximum Irradiance In Angular Range, power per unit area (milliwatts per square centimeter). The optical power delivered to the detector by a source operating at the Maximum Intensity In Angular Range at **Minimum Link Length** must not cause receiver overdrive distortion and possible related link errors. If placed at the Active Output Interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER) specification.

Minimum Irradiance In Angular Range, power per unit area (milliwatts or microwatts per square centimeter). The receiver must meet the BER specification while the source is operating at the Minimum Intensity in Angular Range into the minimum Half-Angle Range at the maximum Link Length.

Half-Angle (degrees) is the half angle of the cone whose apex is at the center of the optical port and whose axis is normal to the surface of the port. The receiver must operate at the Minimum Irradiance In Angular Range from 0 angular degrees (normal to the optical port) to at least the minimum angular range value.

Receiver Latency Allowance (milliseconds or microseconds) is the maximum time after a node ceases transmitting before the node's receiver recovers its specified sensitivity.

Edge Jitter, %. The receiver must allow the link to operate within the specified BER for all possible combinations of output interface specs, except for non-allowed codes. No separate input interface jitter parameters are specified. The actual definitions for the various data rates are given in Section 1.4.2.

2. General Description

2.1. Point-to-Point Link Overview

The serial infrared link supports optical link lengths from zero to at least 1 meter with standard power transceivers (20cm for low power transceivers: see section 4.1) for accurate (within specified bit error ratio), free space communication between two independent nodes (such as a calculator and a printer, or two computers).

2.2. Environment

The Optical Interface Specifications apply over the life of the product and over the applicable temperature range for the product. Background light and electric field test conditions are presented in Appendix A.

2.3. Modulation Schemes

For data rates up to and including 1.152 Mbit/s, RZI modulation scheme is used, and a "0" is represented by a light pulse. For rates up to and including 115.2 kbit/s, the optical pulse duration is nominally 3/16 of a bit duration (or 3/16 of a 115.2 kbit/s bit duration). For 0.576 Mbit/s and 1.152 Mbit/s, the optical pulse duration is nominally 1/4 of a bit duration.

For 4.0 Mbit/s, the modulation scheme is 4PPM. In it, a pair of bits is taken together and called a data symbol. It is divided into 4 "chips", only one of which contains an optical pulse. For 4.0 Mbit/s, the nominal pulse duration (chip duration) is 125 ns. A "1" is represented by a light pulse.

For 16.0 Mbit/s transmission, the HHH(1, 13) code — a low duty cycle, rate 2/3, (d, k) = (1, 13) run-length limited (RLL) code — is used as the modulation code to achieve the specified data rate. The HHH(1, 13) code guarantees for at least one empty chip and at most 13 empty chips between chips containing pulses in the transmitted IR signal.

The 16.0 Mbit/s rate packet frame structure is based on the current IrDA-FIR (4.0 Mbit/s) frame format with modifications introduced where necessary to accommodate the requirements that are specific to the new modulation code. Furthermore, the HHH(1,13) code is enhanced with a simple scrambling/descrambling scheme to further optimize the duty cycle.

2.4. Eye Safety Standards

In the October 1993 edition of IEC 60825-1, LEDs were included along with lasers. The standard requires classification of the Allowable Emission Level of all final products. Allowable emission level refers to the level of ultraviolet, visible or infrared electromagnetic radiation emitted from a product to which a person could be exposed. The IEC standard 60825-1 is amended on 16 Oct 2000 revising the Class 1 eye safety limit and proposing a new Class 1M safety level.

While it is the CENELEC standard which requires regulatory compliance in CENELEC's European member countries, its standard is based on the IEC standard. Because of delays, the CENELEC amendment was approved and is in effect before the IEC amendment. At this time, regulation of LED output is only in effect in the CENELEC countries (most of Europe).

Any product which emits radiation in excess of AEL Class 1 must be labeled (a hazard symbol and an explanatory label would be required). Class 1 products must only be declared as such in the product literature.

Compliance with the IrDA specification does not imply compliance with the IEC and CENELEC standards. Two issues must be addressed. First, the allowed output radiant intensity is a strong function of apparent emitter size (see Appendix A for measurement information). A sufficiently small source could be above Class 1 and still be below the maximum radiant intensity allowed by the specification. Second, the classification must be done under the worst reasonable single fault condition.

3. Media Interface Description

3.1. Physical Representation

A block diagram of one end of a serial infrared link is shown in Figure 2. Additional signal paths may exist. Because there are many implementation alternatives, this specification only defines the serially encoded optical output and input signals at [3].

In the diagram, the electrical signals to the left of the Encoder/Decoder at [1] are serial bit streams. For data rates up to and including 1.152 Mbit/s, the optical signals at [3] are bit streams with a "0" being a pulse, and a "1" is a bit period with no pulse. For 4.0 Mbit/s, a 4PPM encoding scheme is used, with a “1” being a pulse and a “0” being a chip with no pulse. For 16.0 Mbit/s, a HHH(1,13), (d,k) = (1,13) run length limited (RLL), low duty cycle, rate 2/3 modulation code is used. The HHH (1,13) code guarantees for at least one empty chip and at most 13 empty chips between chips containing pulses in the transmitted IR signal. A summary of pulse durations for all supported data rates appears in Table 2 in Section 4.1.

The electrical signals at [2] are the electrical analogs of the optical signals at [3]. For data rates up to and including 115.2 kbit/s, in addition to encoding, the signal at [2] is organized into frames, each byte asynchronous, with a start bit, 8 data bits, and a stop bit. An implementation of this (up to 115.2 kbit/s) is described in Appendix B. For data rates above 115.2 kbit/s, data is sent in synchronous frames consisting of many data bytes. Detail of the frame format is found in Section 5.

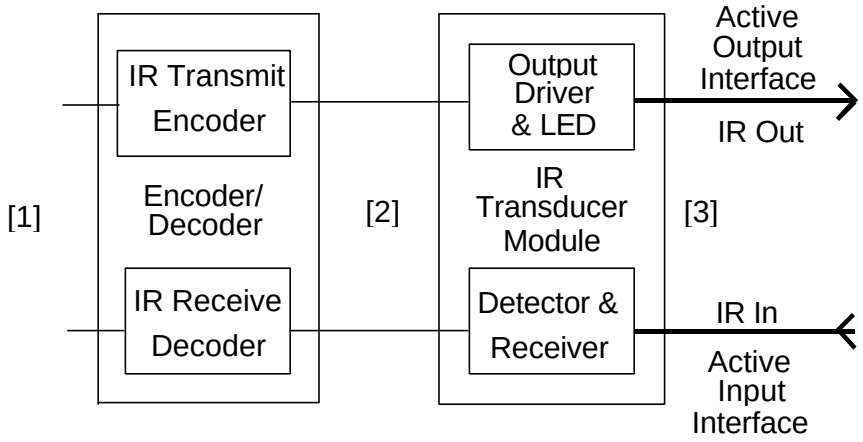


Figure 2. IR Transducer Module

3.2. Optical Angle Definitions

The optical axis is assumed to be normal to the surface of the node's face that contains the optical port (See Figure 3). For convenience, the center of the optical port is taken as the reference point where the optical axis exits the port. If there is asymmetry, as long as the maximum half angle of the distribution is not greater than the allowable Half-Angle Range maximum, and the minimum half angle of the distribution is not less than the Half-Angle Range minimum, the Half-Angle Range specification is met.

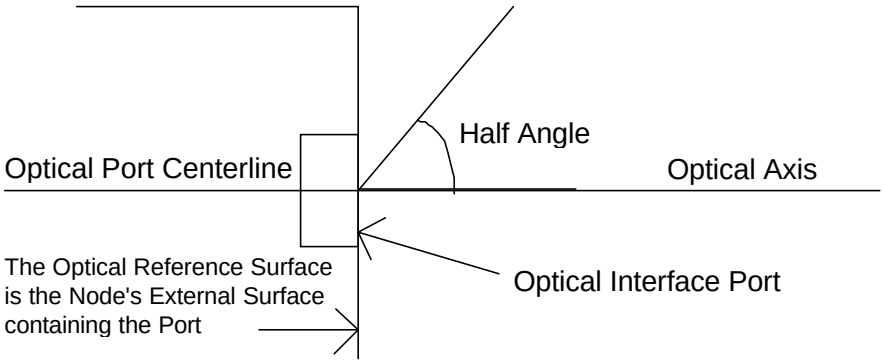


Figure 3. Optical Port Geometry

4. Media Interface Specifications

4.1. Overall Links

There are two different sets of transmitter/receiver specifications. The first, referred to as Standard, is for a link which operates from 0 to at least 1 meter. The second, referred to as the Low Power Option, has a shorter operating range. There are three possible links (See Table 1 below): Low Power Option to Low Power Option, Standard to Low Power Option; Standard to Standard. The distance is measured between the optical reference surfaces.

	Low Power - Low Power	Standard - Low Power	Standard - Standard
Link Distance Lower Limit, meters	0	0	0
Minimum Link Distance Upper Limit, meters	0.2	0.3	1.0

Table 1. Link Distance Specifications

The **Bit Error Ratio** (BER) shall be no greater than 10^-8. The link shall operate and meet the BER specification over its range.

Signaling Rate and Pulse Duration: An IrDA serial infrared interface must operate at 9.6 kbit/second. Additional allowable rates listed below are optional. Signaling rate and pulse duration specifications are shown in Table 2.

For all signaling rates up to and including 115.2 kbit/s the minimum pulse duration is the same (the specification allows both a 3/16 of bit duration pulse and a minimum pulse duration for the 115.2 kbit/s signal (1.63 microseconds minus the 0.22 microsecond tolerance)). The maximum pulse duration is 3/16 of the bit duration, plus the greater of the tolerance of 2.5% of the bit duration, or 0.60 microseconds.

For 0.576 Mbit/s and 1.152 Mbit/s, the maximum and minimum pulse durations are the nominal 25% of the bit duration plus 5% (tolerance) and minus 8% (tolerance) of the bit duration.

For 4.0 Mbit/s, the maximum and minimum single pulse durations are the nominal 25% of the symbol duration plus and minus a tolerance of 2% of the symbol duration. For 4.0 Mbit/s, the maximum and minimum double pulse durations are 50% of the symbol plus and minus a tolerance of 2% of the symbol duration. Double pulses may occur whenever two adjacent chips require a pulse.

For 16 Mbit/s, the maximum and minimum single pulse durations are the nominal symbol duration plus and minus a tolerance of 8% of the nominal symbol duration.

The link must meet the BER specification over the link length range and meet the optical pulse constraints.

Signaling Rate	Modulation	Rate Tolerance % of Rate	Pulse Duration Minimum	Pulse Duration Nominal	Pulse Duration Maximum
2.4 kbit/s	RZI	+/- 0.87	1.41 µs	78.13 µs	88.55 µs
9.6 kbit/s	RZI	+/- 0.87	1.41 µs	19.53 µs	22.13 µs
19.2 kbit/s	RZI	+/- 0.87	1.41 µs	9.77 µs	11.07 µs
38.4 kbit/s	RZI	+/- 0.87	1.41 µs	4.88 µs	5.96 µs
57.6 kbit/s	RZI	+/- 0.87	1.41 µs	3.26 µs	4.34 µs
115.2 kbit/s	RZI	+/- 0.87	1.41 µs	1.63 µs	2.23 µs
0.576 Mbit/s	RZI	+/- 0.1	295.2 ns	434.0 ns	520.8 ns
1.152 Mbit/s	RZI	+/-0.1	147.6 ns	217.0 ns	260.4 ns
4.0 Mbit/s (single pulse) (double pulse)	 4PPM 4PPM	 +/-0.01 +/-0.01	 115.0 ns 240.0 ns	 125.0 ns 250.0 ns	 135.0 ns 260.0 ns
16.0 Mbit/s	HHH(1,13)	+/-0.01	38.3 ns	41.7 ns	45.0 ns

Table 2. Signaling Rate and Pulse Duration Specifications

In order to guarantee non-disruptive coexistence with slower (115.2 kbit/s and below) systems, once a higher speed (above 115.2 kbit/s) connection has been established, the higher speed system must emit a **Serial Infrared Interaction Pulse (SIP)** at least once every 500 ms as long as the connection lasts to quiet slower systems that might interfere with the link. A SIP is defined as a 1.6 µs optical pulse of the transmitter followed by a 7.1 µs off time of the transmitter. It simulates a start pulse, causing the potentially interfering system to listen for at least 500 ms. See Section 5.2.

The specified values for **Rise Time Tr**, **Fall Time Tf**, and **Jitter** are listed in Table 3.

Receiver Latency Allowance and Conditioning: The receiver electronics can become biased (or even saturated) from optical power coupled from the adjacent transmitter LED in the node. If the link is operating near the minimum optical irradiance condition (see Table 4), there may be a significant period of time before the receiver relaxes to its specified sensitivity. This duration includes all aspects of a node changing from transmit to receive. See IrDA (Infrared Data Association) Serial Infrared Link Access Protocol (IrLAP) for negotiation of shorter latency times.

For latency critical applications, such as voice transmission as specified in (IrDA IrMC Specification Version 1.0.1), a low power option module will not interoperate at the maximum link distance with a standard module whose minimum latency is greater than 0.50 milliseconds. For applications where latency is not critical (where latency may be negotiated to a value greater than 0.50 ms), interoperation is possible within the appropriate distance specification.

Receivers with gain control or other adaptive circuitry may require conditioning after durations of no optical input. The protocol allows for additional start flags (STAs) to be used for conditioning.

Link Access and Management Control protocols are covered in separate specification documents (see Section 1.2., References).

4.2. Active Output Interface

At the Active Output Interface, an infrared signal is emitted. The specified Active Output Interface parameters appearing in Table 3 are defined in section 1.4 and the associated test methods are found in Appendix A. Std refers to the standard 0 to 1 meter link; LP refers to the Low Power Option; Both refers to both.

SPECIFICATION	Data Rates	Type	Minimum	Maximum
Peak Wavelength, Up, um	All	Both	0.85	0.90
Maximum Intensity In Angular Range, mW/sr	All	Std	-	500*
" " " " " "		LP	-	72*

Minimum Intensity In Angular Range, mW/sr	115.2 kbit/s & below	Std	40	-
" " " " " "	115.2 kbit/s & below	LP	3.6	-
" " " " " "	Above 115.2 kbit/s	Std	100	-
" " " " " "	Above 115.2 kbit/s	LowPwr	9	-
Half-Angle, degrees	All	Both	15	30
Signaling Rate (also called Clock Accuracy)	All	Both	See Table 2	See Table 2
Rise Time Tr, 10-90%, Fall Time Tf, 90-10% , ns	115.2 kbit/s & below	Both	-	600
Rise Time Tr, 10-90%, Fall Time Tf, 90-10%, ns	> 115.2 kbit/s to 4.0 Mbit/s	Std	-	40
Rise Time Tr, 10-90%, Fall Time Tf, 90-10%, ns	16.0 Mbit/s	Both	-	19
Pulse Duration	All	Both	See Table 2	See Table 2
Optical Over Shoot, %	All	Both	-	25
Edge Jitter, % of nominal pulse duration	115.2 kbit/s & below	Both	-	+/-6.5
Edge Jitter Relative to Reference Clock, % of nominal bit duration	0.576 & 1.152 Mbit/s	Both	-	+/-2.9
Edge Jitter, % of nominal Chip duration	4.0 Mbit/s	Both	-	+/-4.0
Edge Jitter, % of nominal Chip duration	16.0 Mbit/s	Std	-	+/-4.0

* For a given transmitter implementation, the IEC 60825-1 AEL Class 1 limit may be less than this. See section 2.4 above and Appendix A.

Table 3. Active Output Specifications

4.3. Active Input Interface

If a suitable infrared optical signal impinges upon the Active Input Interface, the signal is detected, conditioned by the receiver circuitry, and output to the IR Receive Decoder. The specified Active Input Interface parameters appearing in Table 4 are defined in section 1.4. The test methods for determining the values for a particular serial infrared interface are found in Appendix A.

SPECIFICATION	Data Rates	Type	Minimum	Maximum
Maximum Irradiance In Angular Range, mW/cm^2	All	Both	-	500
Minimum Irradiance In Angular Range, µW/cm^2	115.2 kbit/s & below	LP	9.0	-
" " " " " "	115.2 kbit/s & below	Std	4.0	-
" " " " " "	Above 115.2 kbit/s	LP	22.5	-
" " " " " "	Above 115.2 kbit/s	Std	10.0	-
Half-Angle, degrees	All	Both	15	-
Receiver Latency Allowance, ms	4.0 Mbit/s & below	Std	-	10
Receiver Latency Allowance, ms	4.0 Mbit/s & below	LP	-	0.5
Receiver Latency Allowance, ms	16.0 Mbit/s	Both	-	0.10

Table 4. Active Input Specifications

There is no Half-Angle maximum value for the Active Input Interface. The link must operate at angles from 0 to at least 15 degrees.

There are no Active Input Interface Jitter specifications, beyond that implied in the Active Output Requirements. The link must meet the BER specification for all negotiated and allowable combinations of Active Output Interface specifications, except for non-allowed codes. For rates up to and including 115.2 kbit/s, the allowed codes are described in Infrared Data Association Serial Infrared Link Access Protocol (IrLAP), and Infrared Data Association Link Management Protocol. See Section 1.2, References. For 0.576 Mbit/s and 1.152 Mbit/s and 4.0 Mbit/s, see Section 5 of this document.

5. 0.576 Mbit/s, 1.152 Mbit/s, 4.0 Mbit/s and 16.0 Mbit/s Modulation and Demodulation

5.1. Scope

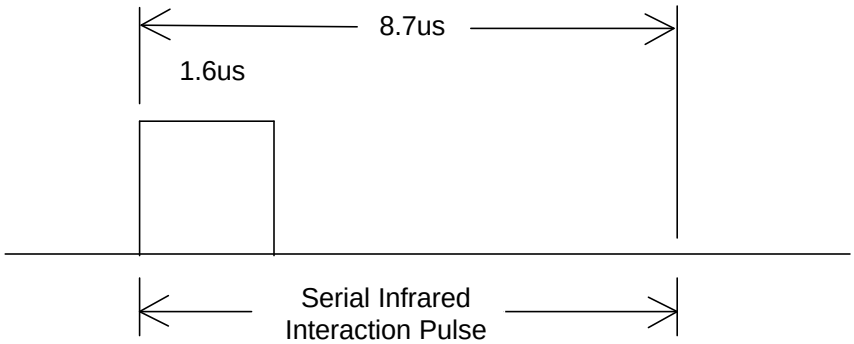
This section covers data modulation and demodulation above 115.2 kbit/s up to 16.0 Mbit/s data rates. The 0.576 Mbit/s and 1.152 Mbit/s rates use an encoding scheme similar to 115.2 kbit/s; the 4.0 Mbit/s rate uses a pulse position modulation (PPM) scheme. Both cases specify packet format, data encoding, cyclic redundancy check, and frame format for use in communications systems based on the optical interface specification.

The 16.0 Mbit/s rate uses the HHH(1,13) encoding scheme with the CRC check and frame format of 4.0 Mbit/s rate with necessary modfications to the frame format for the new modulation code.

Systems operating at these higher rates are transparent to IrLAP and IrLMP as it is defined for the lower rates. Architecturally, it appears as an alternate modulation/demodulation (modem) path for data from IrLAP bound for the IR medium. These higher rates are negotiated during normal IrLAP discovery processes. For these and specific discovery bit field definitions of the higher rates, see documents referenced in Section 1.2.

5.2. Serial Infrared Interaction Pulses

In order to guarantee non-disruptive coexistence with slower (up to 115.2 kbit/s) systems, once a higher speed (above 115.2 kbit/s) connection has been established, the higher speed system must emit a **Serial infrared Interaction Pulse (SIP)** at least once every 500 ms as long as the connection lasts to quiet slower systems that might interfere with the link (see Section 4.1). The pulse can be transmitted immediately after a packet has been transmitted. The pulse is shown below:



5.3. 0.576 Mbit/s and 1.152 Mbit/s Rates

5.3.1. Encoding

The 0.576 Mbit/s and 1.152 Mbit/s encoding scheme is similar to that of the lower rates except that it uses one quarter pulse duration of a bit cell instead of 3/16, and uses HDLC bit stuffing after five consecutive ones instead of byte insertion. The following illustrates the order of encoding.

1) The raw transmitted data is scanned from the least significant to the most significant bit of each byte sent and a 16 bit CRC-CCITT is computed for the whole frame except flags and appended at the end of data.

The CRC-CCITT polynomial is defined as follows:

$$CRC(x) = x^{16} + x^{12} + x^{5} + 1$$

(For an example refer to the 32 bit CRC calculation in section 5.4.2.5 and adjust the polynomial for the one indicated above and note the size will be 16 bits (2 bytes) instead of 32 bits (4 bytes) , note preset to all 1's and inversion of the outgoing CRC value)

(The address and control field are considered as part of data in this example.) For example, say four bytes, 'CC'hex, 'F5'hex, 'F1'hex, and 'A7'hex, are data to be sent out in sequence, then '51DF'hex is the CRC-CCITT.

LSB MSB
Raw Data 00110011 10101111 10001111 11100101

LSB MSB
Data/CRC 00110011 10101111 10001111 11100101 11111011 10001010

2) A 'Zero' is inserted after five consecutive ones are transmitted in order to distinguish the flag from data. Zero insertion is done on every field except the flags. Using the same data as an example;

LSB MSB
Data/CRC 00110011 10101111 10001111 11100101 11111011 10001010

First bit to be transmitted Last bit to be transmitted
Transmit Data 00110011101011111000011111011001011111010111000101001111110

(Note: Underlined zeros are inserted bits.)

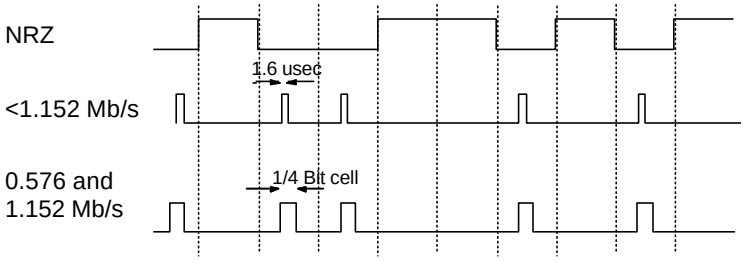
3) The beginning and ending flags, '7E'hex, are appended at the beginning and end. Using the same example;

First bit to be transmitted Last bit to be transmitted
Transmit Data 01111110001100111010111110000111110110010111110101110001010011111110

4) An additional beginning flag is added at the beginning. Finally the whole frame to be sent out is:

First bit to be transmitted Last bit to be transmitted
Tx Frame 01111110011111100011001110101111100001111101100101111101011100010100111111 10

5) The transmitter sends out 1/4-bit-cell-length pulse of infrared signal whenever data is zero. For example, the frame to be sent out is 0100110101 in binary in the order of being transmitted, then the following figure illustrates the actually transmitted signal for lower data rates and also for 0.576 and 1.152 Mbit/s.



5.3.2. Frame Format

5.3.2.1. Frame Overview

The 0.576 Mbit/s and 1.152 Mbit/s frame format follows the standard HDLC format except that it requires two beginning flags and consists of two beginning flags, an address field, a control field, an information field, a frame check sequence field and minimum of one ending flag. ‘7E’hex is used for the beginning flag as well as for the ending flag. The frame format is the same as for the lower rate IrLAP frame with STA changed from ‘C0’hex to ‘7E’hex and STO changed from ‘C1’hex to ‘7E’hex.

STA: Beginning Flag, 01111110 binary
ADDR: 8 bit Address Field
DATA: 8 bit Control Field plus up to 2045 = (2048 - 3) bytes Information Field
FCS: CCITT 16 bit CRC
STO: Ending Flag, 01111110 binary

Note 1: Minimum of three STO fields between back to back frames is required.
Note 2: Zero insertion after five consecutive 1's is used. CRC is computed before zero insertion is performed.
Note 3: Least significant bit is transmitted first.
Note 4: Abort sequence requires minimum of seven consecutive 1’s.
Note 5: 8 bits are used per character before zero insertion.

5.3.2.2. Beginning Flag (STA) and Ending Flag (STO) Definition

The 0.576 Mbit/s and 1.152 Mbit/s links use the same physical layer flag, 01111110, for both STA and STO. It is required to have a minimum of two STAs and a minimum of one STO. The receiver treats multiple STAs or STOs as a single flag even if it receives more than one.

5.3.2.3. Address Field (ADDR) Definition

The 0.576 Mbit/s and 1.152 Mbit/s links expect the first byte after STA to be the 8 bit address field. This address field should be used as specified in the IrLAP.

5.3.2.4. Data Field (DATA) Definition

The data field consists of Control field and optional information field as defined in the IrLAP.

5.3.2.5. Frame Check Sequence Field (FCS) Definition

The 0.576 Mbit/s and 1.152 Mbit/s links use a 16 bit CRC-CCITT cyclic redundancy check to check received frames for errors that may have been introduced during frame transmission. The CRC is computed from the ADDR and Data fields using the same algorithm as specified in the IrLAP.

5.3.2.6. Frame Abort

A prematurely terminated frame is called an aborted frame. The frame can be aborted by blocking the IR transmission path in the middle of the frame, a random introduction of infrared noise, or intentional termination by the transmitter. Regardless what caused the aborted frame, the receiver treats a frame as an aborted frame when seven or more consecutive ones (no optical signal) are received. The abort terminates the frame immediately without the FCS field or an ending flag.

5.3.2.7. Frame Transmission Order

All fields are transmitted the least significant bit of each byte first.

5.3.2.8. Back to Back Frame Transmission

Back to back, or “brick-walled” frames are allowed with three or more flags, ‘01111110’b, in between. If two consecutive frames are not back to back, the gap between the last ending flag of the first frame and the STA of the second frame should be separated by at least seven bit durations (abort sequence).

5.4. 4 Mbit/s Rate

5.4.1. 4PPM Data Encoding Definition

Pulse Position Modulation (PPM) encoding is achieved by defining a data symbol duration (Dt) and subsequently subdividing Dt into a set of equal time slices called "chips." In PPM schemes, each chip position within a data symbol represents one of the possible bit combinations. Each chip has a duration of Ct given by:

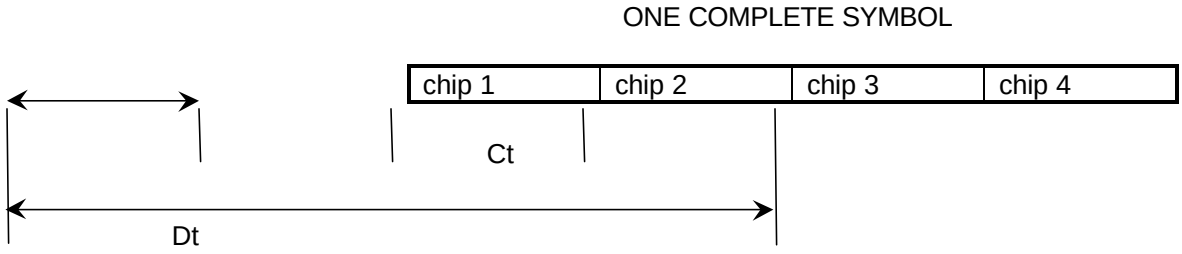
Ct = Dt/Base

In this formula "Base" refers to the number of pulse positions, or chips, in each data symbol. The Base for IrDA PPM 4.0 Mbit/s systems is defined as four, and the resulting modulation scheme is called "four pulse position modulation (4PPM)." The data rate of the IrDA PPM system is defined to be 4.0 Mbit/s. The resulting values for Ct and Dt are as follows:

Dt = 500 ns

Ct = 125 ns

The figure below describes a data symbol field and its enclosed chip durations for the 4PPM scheme.

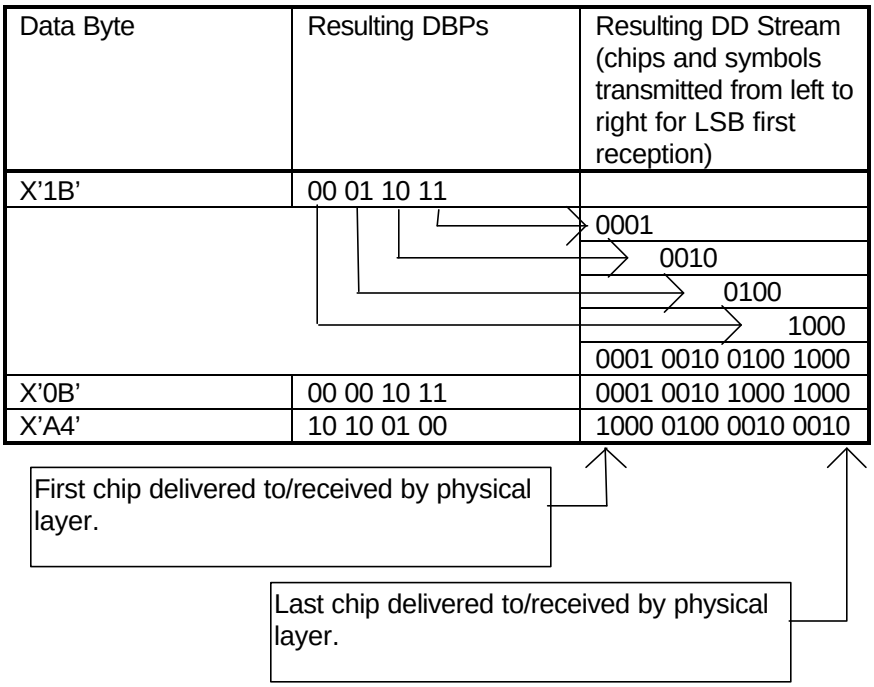


Because there are four unique chip positions within each symbol in 4PPM, four independent symbols exist in which only one chip is logically a "one" while all other chips are logically a "zero." We define these four unique symbols to be the only legal data symbols (DD) allowed in 4PPM. Each DD represents two bits of payload data, or a single "data bit pair (DBP)", so that a byte of payload data can be represented by four DDs in sequence. The following table defines the chip pattern representation of the four unique DDs defined for 4PPM.

Data Bit Pair (DBP)	4PPM Data Symbol (DD)
00	1000
01	0100
10	0010
11	0001

Logical “1” represents a chip duration when the transmitting LED is emitting light, while logical “0” represents a chip duration when the LED is off.

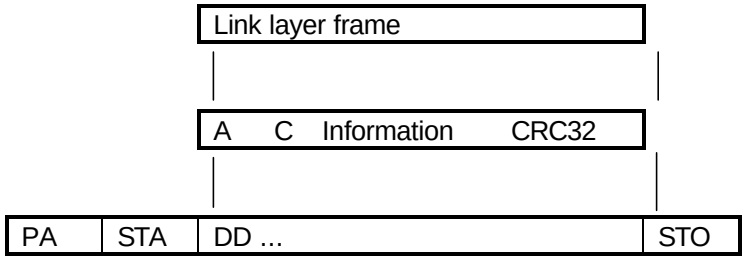
Data encoding for transmission is done LSB first. The following examples show how various data bytes would be represented after encoding for transmission. In these examples transmission time increases from left to right so that chips and symbols farthest to the left are transmitted first.



5.4.2. PPM Packet Format

5.4.2.1. Packet Overview

For 4.0 Mbit/s PPM packets the following packet format is defined:

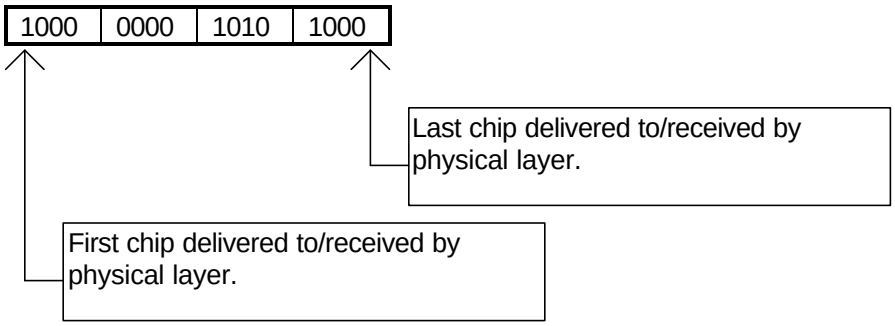


In this packet format, the payload data is encoded as described in the 4PPM encoding above, and the encoded symbols reside in the DD field. Maximum packet length is negotiated by the same mechanism as for the slower rates. The preamble field (PA) is used by the receiver to establish phase lock. During PA, the receiver begins to search for the start flag (STA) to establish symbol synchronization. If STA is received correctly, the receiver can begin to interpret the data symbols in the DD field. The receiver continues to receive and interpret data until the stop flag (STO) is recognized. STO indicates the end of a frame. The chip patterns and symbols for PA, STA, FCS field, and STO are defined below. Only complete packets that contain the entire format defined above are guaranteed to be decoded at the receiver (note that, as for the lower rates, the information field, I, may be of zero length).

The 4PPM data encoding described above defines only the legal encoded payload data symbols. All other 4 chip combinations are by definition illegal symbols for encoded payload data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag fields because they are unambiguously not data.

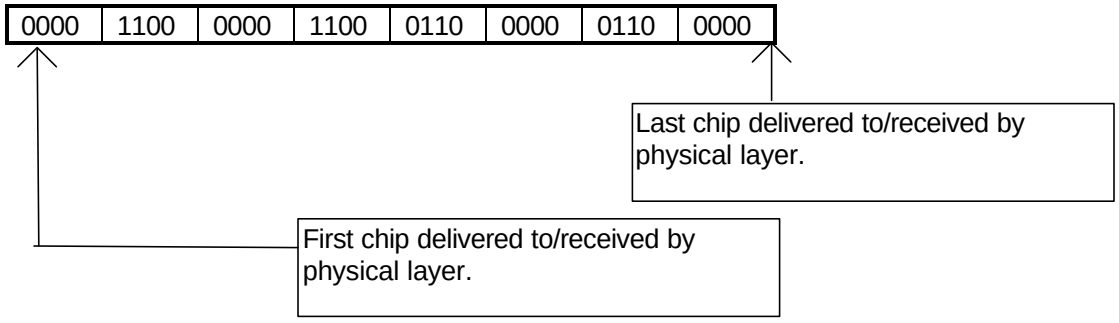
5.4.2.2. Preamble Field Definition

The preamble field (PA) consists of exactly sixteen repeated transmissions of the following stream of symbols. In the PA field, transmission time increases from left to right so that chips and symbols on the left are transmitted first.



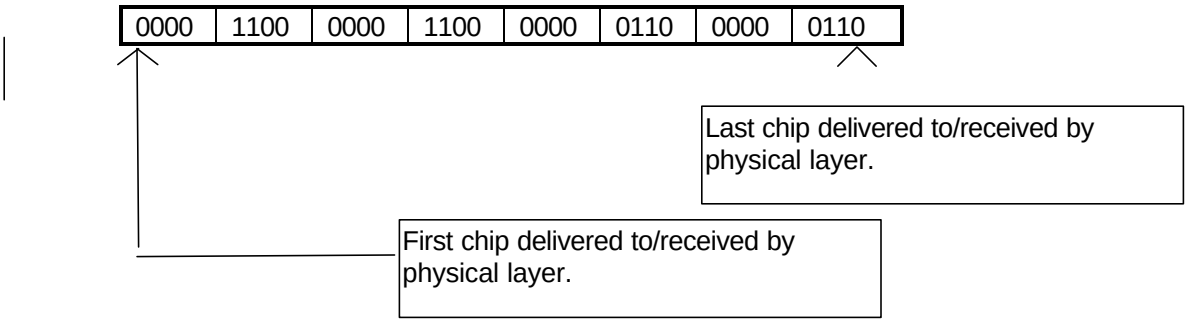
5.4.2.3. Start Flag Definition

The start flag (STA) consists of exactly one transmission of the following stream of symbols. In the STA field, transmission time increases from left to right so that chips and symbols on the left are transmitted first.



5.4.2.4. Stop Flag Definition

The stop flag (STO) consists of exactly one transmission of the following stream of symbols. In the STO field, transmission time increases from left to right so that chips and symbols on the left are transmitted first.



5.4.2.5. Frame Check Sequence Field Definition

Frame check sequence (FCS) field is a 32 bit field that contains a cyclic redundancy check (CRC) value. The CRC is a calculated, payload data dependent field, calculated before 4 PPM encoding. It consists of the 4PPM encoded data resulting from the IEEE 802 CRC32 algorithm for cyclic redundancy check as applied to the payload data contained in the packet. The CRC32 polynomial is defined as follows:

$$CRC(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

The CRC32 calculated result for each packet is treated as four data bytes, and each byte is encoded in the same fashion as is payload data. Payload data bytes are input to this calculation in LSB first format.

The 32 bit CRC register is preset to all "1's" prior to calculation of the CRC on the transmit data stream. When data has ended and the CRC is being shifted for transmission at the end of the packet, a "0" should be shifted in so that the CRC register becomes a virtual shift register. Note: the inverse of the CRC register is what is shifted as defined in the polynomial. An example of a verilog implementation follows to describe the process.

```
module txcrc32(clrcrc,clk,txdin,nreset,crcndata,txdout,bdcrc);
/* ************************************************************************** */
// compute 802.X CRC x32 x26 x23 x22 x16 x12 x11 x10 x8 x7 x5 x4 x2 x + 1
// on serial bit stream.
/* ************************************************************************** */
/* bdcrc is input signal used to send a bad crc for test purposes */
/* note ^ is exclusive or function */

input clrcrc,clk,txdin,nreset,crcndata,bdcrc;
output txdout;
reg [31:0] nxtxcrc,txcrc;

/* ************************************************************************** */
// XOR data stream with output of CRC register and create input stream
// if crcndata is low, feed a 0 into input to create virtual shift reg
/* ************************************************************************** */

wire crcshin = (txcrc[31] ^ txdin) & ~crcndata;

/* ************************************************************************** */
// combinatorial logic to implement polynomial
/* ************************************************************************** */

always @ (txcrc or clrcrc or crcshin)
begin
if (clrcrc)
nxtxcrc <= 32'hffffffff;
else
begin
nxtxcrc[31:27] <= txcrc[30:26];
nxtxcrc[26] <= txcrc[25] ^ crcshin; // x26
nxtxcrc[25:24] <= txcrc[24:23];
nxtxcrc[23] <= txcrc[22] ^ crcshin; // x23
nxtxcrc[22] <= txcrc[21] ^ crcshin; // x22
nxtxcrc[21:17] <= txcrc[20:16];
nxtxcrc[16] <= txcrc[15] ^ crcshin; // x16
nxtxcrc[15:13] <= txcrc[14:12];
nxtxcrc[12] <= txcrc[11] ^ crcshin; // x12
nxtxcrc[11] <= txcrc[10] ^ crcshin; // x11
nxtxcrc[10] <= txcrc[9] ^ crcshin; // x10
nxtxcrc[9] <= txcrc[8];
```

```
nxtxcrc[8] <= txcrc[7] ^ crcshin; // x8
nxtxcrc[7] <= txcrc[6] ^ crcshin; // x7
nxtxcrc[6] <= txcrc[5];
nxtxcrc[5] <= txcrc[4] ^ crcshin; // x5
nxtxcrc[4] <= txcrc[3] ^ crcshin; // x4
nxtxcrc[3] <= txcrc[2];
nxtxcrc[2] <= txcrc[1] ^ crcshin; // x2
nxtxcrc[1] <= txcrc[0] ^ crcshin; // x1
nxtxcrc[0] <= crcshin; // +1
end

end

/* ********************************************************************** */
// infer 32 flops for storage, include async reset asserted low
/* ********************************************************************** */
always @ (posedge clk or negedge nreset)
begin
if (!nreset)
txcrc <= 32'hffffffff;
else
txcrc <= nxtxcrc;     // load D input (nxtxcrc) into flops
end

/* ********************************************************************** */
// normally crc is inverted as it is sent out
// input signal badcrc is asserted to append bad CRC to packet for
// testing, this is an implied mux with control signal crcndata
// if crcndata = 0 , the data is passed by unchanged, if = 1 then
// the crc register is inverted and transmitted.
/* ********************************************************************** */

wire txdout = (crcndata) ? (~txcrc[31] ^ bdcrc) : txdin; // don't invert
                                                         // if bdcrc is 1
endmodule
/* ********************************************************************** */
```

The following shows a CRC calculation and how the results would be represented after encoding for transmission. The results of the CRC calculation (txcrc[31 - 0]) is shown in the next table when the contents of the DD field is X'1B' and X'A4', where X'1B' is the first byte of the DD field. If the four bytes of CRC are counted as received data, then the resultant 6 bytes in order would be X'1B', X'A4', X'94', X'BE', X'54' and X'39'.

	[31] [0]
txcrc[31-0]	1101 0110 1000 0010 1101 0101 0110 0011
~txcrc[31-0]	0010 1001 0111 1101 0010 1010 1001 1100

CRC Value	Resulting DBPs	Resulting DD Stream (chips and symbols transmitted from left to right for LSB first reception)
~txcrc[24-31]	10 01 01 00	
		1000
		0100
		0100
		0010
		1000 0100 0010 0001
~txcrc[16-23]	10 11 11 10	0010 0001 0001 0010
~txcrc[8-15]	01 01 01 00	1000 0100 0100 0100
~txcrc[0-7]	00 11 10 01	0100 0010 0001 1000

First chip delivered to/received by physical layer.

Last chip delivered to/received by physical layer.

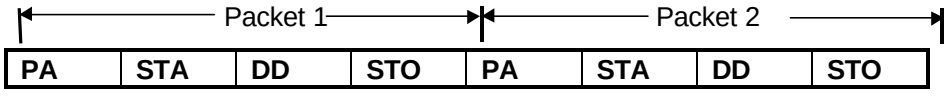
5.4.3. Aborted Packets

Receivers may only accept packets that have valid STA, DD, FCS, and STO fields as defined in the PPM Packet Format section. The PA field need not be valid in the received packet. All other packets are aborted and ignored.

Any packet may be aborted at any time after a valid STA but before transmission of a complete STO flag by two or more repeated transmissions of the illegal symbol "0000." Also, any packet may be aborted at any time after a valid STA by reception of any illegal symbol which is not part of a valid STO field.

5.4.4. Back to Back Packet Transmission

Back to back, or "brick-walled" packets are allowed, but each packet must be complete (i.e., containing PA, STA, DD and STO fields). Brick-walled packets are illustrated below.



5.5 16.0 Mbit/s Rate

The 16.0 Mbit/s data transmission is evolved with no changes to the link distance, bit error ratio, half angle, field of view, minimum and maximum intensity levels and minimum and maximum irradiance levels. It incorporates a new modulation code HHH (1,13) – low duty cycle, rate 2/3, (d,k) = (1, 13) run-length limited (RLL) code to achieve the specified data rate. The HHH(1,13) code guarantees for at least one empty chip and at most 13 empty chips between chips containing pulses in the transmitted IR signal.
The data transmission packet/ frame is based on 4.0 Mbit/s frame format with modifications introduced where necessary to accommodate the requirements that are specific to the new modulation code. The system includes a simple scrambling/descrambling scheme to randomize the duty cycle statistics. The signaling rate of the 16.0 Mbit/s data rate is 24.0 Mchips/s, where a chip is the smallest element of IrDA signaling.

5.5.1 HHH (1,13) Modulation Code

The HHH(1, 13) modulation code has the following salient features:

- Code Rate: 2/3 ,
- Maximal Duty Cycle: 1/3 (~33%) ,
- Average Duty Cycle: ~26% ,
- Minimal Duty Cycle: 1/12 (~8.3%) ,
- Run-Length Constraints: (d, k) = (1, 13) ,
- Longest Run of '10's: yyy'000'101'010'101'000'yyy ,
- Chip Rate @ Data Rate 16 Mbit/s: 24 Mchips/s ,
- System Clock @ Data Rate 16 Mbit/s: N×12 MHz (where N ≥ 4).

The HHH(1,13) code is a Run Length Limited (RLL) code that provides both power efficiency and bandwidth efficiency at the high data rate. The signaling rate of the code is 24 Mchips/s allowing a rise and fall time of 19 ns. LED on time is further improved by having a 26% average duty cycle for random data. The lower duty cycle is achieved by scrambling the incoming data stream.The run length constraints (d, k) = (1, 13) ensure an inactive chip after each active chip, i.e. only single-chip-width pulses occur. This feature allows a source or a receiver to exhibit a long tail property. To take full advantage of the d = 1 feature of HHH(1, 13) in strong signal conditions, clock and data recovery circuitry should be designed to ignore the level of the chip following an active chip and assume these chips are inactive. The modulation code is enhanced with simple frame-synchronized scrambler/descrambler mechanisms as defined and described in **Section 5.5.4**. While such a scheme does not eliminate worst-case duty cycle signal patterns in all specific cases, the probabilities of their occurrence are reduced signifcantly on average. This leads to a better "eye" opening and reduced jitter in the recovered signal stream for typical payload data.

5.5.2 Data Encoding Definition

The encoding definition of the HHH (1,13) code is provided by a state transition table. The State Transition Table would be typically implemented as a set of boolean logic equations and flip flops. The State Transition Table is described as follows:
The particular HHH(1, 13) code construction and implementation methods require the following interpretation of the table entries with respect to the mapping of Internal Inputs and Present State into Next State and Internal Output, respectively:

- A specific data pair $D \equiv D^* = (\delta 1, \delta 2)$ arriving at the encoder input is first associated with a corresponding next state $N \equiv N^*$. This occurs as soon as the data D* have advanced into the positions of the internal data bits $B^1 = (b1, b2)$, i.e., when $(b1, b2, b3, b4, b5, b6) \equiv (\delta 1, \delta 2, x, x, x, x)$. In a second step, during the next encoding cycle, the state S takes on the value of N*, i.e., $S \equiv S^* \leftarrow N^*$ so that S is now associated with $(\delta 1, \delta 2)$. In the same cycle, the inner codeword $C \equiv C^*$ now carrying the information of D* is computed. Thus, referring to Table 5.5.1, a given internal input vector (b1, b2, b3, b4, b5, b6) associates the bits (b1, b2) with the next state N and a given state S associates the data pair ahead of (b1, b2) to the output C. In other words, the pair-wise values for N and C as listed in Table 5.5.1 are not associated with the same input data pair.

- Encoder initialization: The state S = (s1, s2, s3) = (1, 0, 0) is also used as the initial state of the encoder, i.e., denoting with (α, β) the first pair of data bits to be encoded, the state S is forced to take on the value (1, 0, 0) when the bits (α, β) have advanced into the encoding circuits such that the internal inputs $B^1 = (b1, b2) \equiv (\alpha, \beta)$.

Present State: $S=(s_1, s_2, s_3)$	Next State / Internal Output: $N=(n_1, n_2, n_3)$ / $C=(c_1, c_2, c_3)$							
	Internal Inputs: $(b_1, b_2, b_3, b_4, b_5, b_6)$							
	00xxxx	01xxxx	10xxxx	1100xx	1101xx	111011	1110(~~11~~)	1111xx
0 0 0	000/010	001/010	010/010	111/010	111/001	111/010	011/010	011/010
0 0 1	000/001	001/001	100/001	100/010	100/010	100/010	100/010	100/010
0 1 0	000/100	001/100	010/100	111/100	111/101	111/100	011/100	011/100
0 1 1	000/101	001/101	100/101	100/100	100/100	100/100	100/100	100/100
1 0 0 [1)]	000/000	001/000	010/000	011/000	011/000	011/000	011/000	011/000
1 1 1	100/000	100/000	111/000	100/000	100/000	100/000	100/000	100/000

Table 16. State transition/output table for the HHH(1, 13) code (Note: [1)] the state (s1, s2, s3) = (1, 0, 0) is the required initial state during the one encoding cycle where the internal input pair B^1 = (b1, b2) represents the first data pair to be encoded; 'x' signifies don't care).

The State transition table above can be implemented as a set of encoding equations as below:
Define the following encoder signal vectors where increasing indexes mean increasing time in the equivalent serial signal streams:

Data input *): $D=(d_1, d_2)$

*) First data input to be encoded: $D \equiv \tilde{D}=(\alpha, \beta)$

Present state: $S=(s_1, s_2, s_3)$

Next state: $N=(n_1, n_2, n_3)$

Internal data: $B^1=(B^1{}_1, B^1{}_2)=(b_1, b_2)$

$B^2=(B^2{}_1, B^2{}_2)=(b_3, b_4)$

$B^3=(B^3{}_1, B^3{}_2)=(b_5, b_6)$

Internal codeword: $C=(c_1, c_2, c_3)$

Encoder output: $Y=(Y_1, Y_2, Y_3)$

Initial conditions (start up): $S=(s_1, s_2, s_3)=(1, 0, 0)$ when $B^1=(b_1, b_2) \equiv \tilde{D}=(\alpha, \beta)$

With the Boolean operator notation

$\overline{m}$ = INVERSE (m),
$m+n$ = m OR n,
mn = m AND n,

the components of N and C are computed in terms of the components of S, B^1, B^2, and B^3 with the following Boolean expressions:

$$n_1 = (s_1 s_3) + (s_3 b_1) + (\overline{s_1} b_1 b_2 \overline{b_3}) + (\overline{s_1} b_1 b_2 \overline{b_4} b_5 b_6) ,$$

$$n_2 = (\overline{s_3} b_1) + (s_1 s_2 b_1 \overline{b_2}) ,$$

$$n_3 = (\overline{s_3} b_2) + (\overline{s_1}\ \overline{b_1} b_2) + (s_1 s_2 b_1 \overline{b_2}) ,$$

$$c_1 = \overline{s_1} s_2 ,$$

$$c_2 = \overline{s_1}\ \overline{s_2}\ \overline{c_3} ,$$

$$c_3 = \overline{s_1} s_3 (\overline{b_1} + \overline{b_2}) + (\overline{s_1}\ \overline{s_3} b_1 b_2 \overline{b_3}\ b_4) .$$

The vectors B^1, B^2, B^3, S, and Y are outputs of latches; in every encoding cycle, they are updated as follows:

$$B^1 \leftarrow B^2 \leftarrow B^3 \leftarrow D ,$$

$$S \leftarrow N , \text{ and } Y \leftarrow C .$$

5.5.3 HHH (1,13) Packet Format

5.5.3.1 Packet Overview

The packet format for 16.0 Mbit/s HHH(1,13) has the following form

PREAMBLE (PA)	START (STA)	IrLAP Frame	CRC	Flush Byte (FB)	STOP (STO)	NULL

The payload data is encoded as described in the HHH (1,13) encoding above, and the encoded symbols reside in the IrLAP Frame field. The preamble field (PA) is used by the receiver to establish phase lock. During PA, the receiver begins to search for the start flag (STA) to establish symbol synchronization. If STA is received correctly, the receiver can begin to interpret the data symbols in the IrLAP Frame field. The receiver continues to receive and interpret data until the stop flag (STO) is recognized. STO indicates the end of a frame. The chip patterns and symbols for PA, STA, CRC field, and STO are defined below. Only complete packets that contain the entire format defined above are guaranteed to be decoded at the receiver (note that, as for the lower rates, the information field, I, that is part of the IrLAP field, may be of zero length).

The 16.0 Mbit/s packet contains several fields for the purposes of clock recovery, synchronization and data transmission. In concept, the packet format is similar to that used in 4.0 Mbit/s and thus the existing controller designs can be used at a higher data rate. However, there are specific controller elements like clock recovery, synchronization and encoding/decoding circuits that need to be implemented specifically for 16.0 Mbit/s data rate. The packet engines in the existing controllers can be reused and this will mean gate count and reengineering effort is kept to a minimum.

5.5.3.2 Preamble Field Definition

The transmitted PREAMBLE (PA) is constructed by concatenating ten times (10×) the 24-chip (1 µs) PREAMBLE PERIOD (PP), where

PP = '100'010'010'001'001'001'000'100',

to form the complete 240-chip (10 µs) preamble

PA = 'PP'PP'PP'PP'PP'PP'PP'PP'PP'PP'.

The left-most/right-most chip of PP and PA, respectively, is transmitted first/last and a '1' in PP means an active chip (pulse) and a '0' means an empty chip (no pulse).

5.5.3.3. START (STA) FLAG DEFINITION:

The transmitted START (STA) delimiter is the 48-chip (2 μs) chip sequence

STA = '100'101'010'100'100'010'000'001'001'010'101'001'000'001'010'000'.

The left-most/right-most chip of STA is transmitted first/last and a '1' in STA means an active chip (pulse) and a '0' means an empty chip (no pulse).

The Start Flag Delimiter allows for packet synchronization. A delimiter detection circuit should declare a flag as having been found when there is a perfect match between the receiver chip stream and a particular delimiter. The Start and Stop delimiters contain a subsequence '1001010101001' that violates the HHH (1,13) code. This subsequence occurs twice in the Start Flag delimiter and never occurs within the main HHH code.

5.5.3.4 IrLAP Frame:

The structure remains unchanged from that defined in the IrLAP Specification, Version 1.1. The content of the IrLAP frame is first scrambled with the scheme recommended in Section 5.5.4. and then encoded with HHH(1,13) as described in Section **5.5.2**. Note that the 32 CRC bits for the IrLAP frame are calculated before the IrLAP frame is scrambled. For reference, the IrLAP frame has the following structure:

| Address (8 bits) | Control (8 bits) | Information (M times 8 bits) |

5.5.3.5. CRC:

Computation remains unchanged from the 32-bit CRC defined for the 4 Mbit/s data rate. Please refer Section 5.4.2.5 for this CRC function. The content of the CRC field is first scrambled with the scheme recommended in **Section 5.5.4** and then encoded with HHH(1, 13) as described in **Section 5.5.2**. Note that the 32 CRC bits for the IrLAP frame are calculated before the IrLAP frame is scrambled. The transmitted CRC field is a 48-chip (2 μs) sequence.

5.5.3.6. FLUSH BYTE (FB):

The Flush Byte (FB) is the 8-bit sequence

FB = '00'00'00'00'.

These 8 bits are not scrambled but directly sent to the HHH(1, 13) encoder. The transmitted FB field is a 12-chip (0.5 μs) sequence. Note that the FB field is required to enable complete decoding of the CRC field. The flush byte denotes the end of the main body. Since the flush byte is not scrambled, a well balanced HHH(1,13) sequence precedes the STOP delimiter.

5.5.3.7. STOP (STO):

The transmitted STOP (STO) delimiter is the 48-chip (2 μs) sequence

STO = '001'001'010'101'001'000'100'000'100'101'010'100'100'000'100'000'.

The left-most/right-most chip of STO is transmitted first/last and a '1' in STO means an active chip (pulse) and a '0' means an empty chip (no pulse). As in the Start Flag delimiter, the Stop flag also contains a subsequence '1001010101001' that violates the HHH (1,13) code. This subsequence also occurs twice in the Stop Flag delimiter.

5.5.3.8. NULL sequence:

The transmitted NULL sequence is the 24-chip (1 μs) sequence

NULL = '000'000'000'000'000'000'000'000'.

The NULL field is a new field for the purpose of providing an HHH(1, 13) code pattern violation that permits terminating reception of the packet in the event that the STO field is not recognized. The left-most/right-most chip in NULL is transmitted first/last and all chips of NULL are empty chips (no pulses).

The NULL field increases the probability that the packet is terminated close to the STOP flag. The NULL field also reduces the probability that two back to back packets are interpreted as a single packet, should the STOP flag delimiter of the first packet be missed.

5.5.4 Scrambling and Descrambling Functions

It is advantageous to enhance the encoder/decoder system with simple scrambler/descrambler functions. The primitive polynomial

$$x^8 \oplus x^4 \oplus x^3 \oplus x^2 \oplus 1 ,$$

where $\oplus$ indicates a modulo-2 addition or, equivalently, a logic exclusive OR (XOR) operation, is proposed for implementing these functions. The operations of the proposed scrambling and descrambling functions are performed according to the principles of frame synchronized scrambling/descrambling (FSS) mechanisms. Note that FSS does not introduce memory into the signal path, i.e., FSS does not increase the encoding/decoding delay and it does not aggravate error propagation in the decoded data stream. The hardware used for scrambling during transmission can mostly be reused during the descrambling process in reception mode.

The reference hardware implementation of the proposed scrambling/descrambing scheme is shown in the following figure. The linear feedback shift register (LFSR) produces a maximum-length pseudo-random sequence with period 255. It is important to note that the proposed scrambling/descrambling functions are implemented with an LFSR where the feedback taps are configured according to the so-called one-to-many implementation; for reasons of compatibility, implementations should adhere to this type of LFSR. Furthermore, it is assumed that the output of register cell x6 shown in the figure is defined to be the equivalent serial output of the LFSR.

The modulo-2 adders shown in the figure correspond to logic XOR (exclusive OR) gates. During transmission, each new pair of source bits (d1', d2') is XOR-ed with a new pair of scrambling bits (s1, s2) to produce the scrambled data bit pair (d1, d2) entering the encoder. Similarly, during reception, each new pair of decoded bits (u1, u2) is XOR-ed with a new pair of descrambling bits (s1, s2) to produce the descrambled user bit pair (u1', u2') that is sent to the data sink. A scrambling/descrambling cycle has duration 3T seconds where T = 41.7 ns is the chip period.

5.5.4.1 Effects and Limits of Scrambling/Descrambling:

By enhancing the system with scrambling/descrambling functions during data transmission/reception, one achieves generally better duty cycle statistics in the HHH(1, 13) coded channel chip stream; the resulting duty cycle converges towards the average duty cycle of the code (≈26%) for typical payload data. It is important to note that scrambling cannot entirely eliminate possible worst-case duty cycle patterns in the transmitted signal stream that can result from certain specific input data sequences. However, scrambling can greatly reduce the probability of occurrence of such worst-case patterns.

5.5.4.2 Scrambler/ Descrambler Initialization:

Transmit mode: The scrambler's LFSR is initialized with the all-1 state, that is (x8, x7, x6, x5, x4, x3, x2, x1) = (1, 1, 1, 1, 1, 1, 1, 1), such that (s1, s2) = (x6, x5) = (1, 1) at the arrival of the first pair of source bits (d1', d2'), ready to be scrambled. Note that the LFSR must be advanced *twice* per scrambling cycle to produce a new pair of scrambling bits (s1, s2) for each new pair of data bits (d1', d2').

Receive mode: The descrambler's LFSR is initialized with the all-1 state, that is (x8, x7, x6, x5, x4, x3, x2, x1) = (1, 1, 1, 1, 1, 1, 1, 1), such that (s1, s2) = (x6, x5) = (1, 1) when the decoder produces the first pair of decoded bits (u1, u2), ready to be descrambled. Note that the LFSR must be advanced *twice* per descrambling cycle to produce a new pair of descrambling bits (s1, s2) for each new pair of decoded data bits (u1, u2).

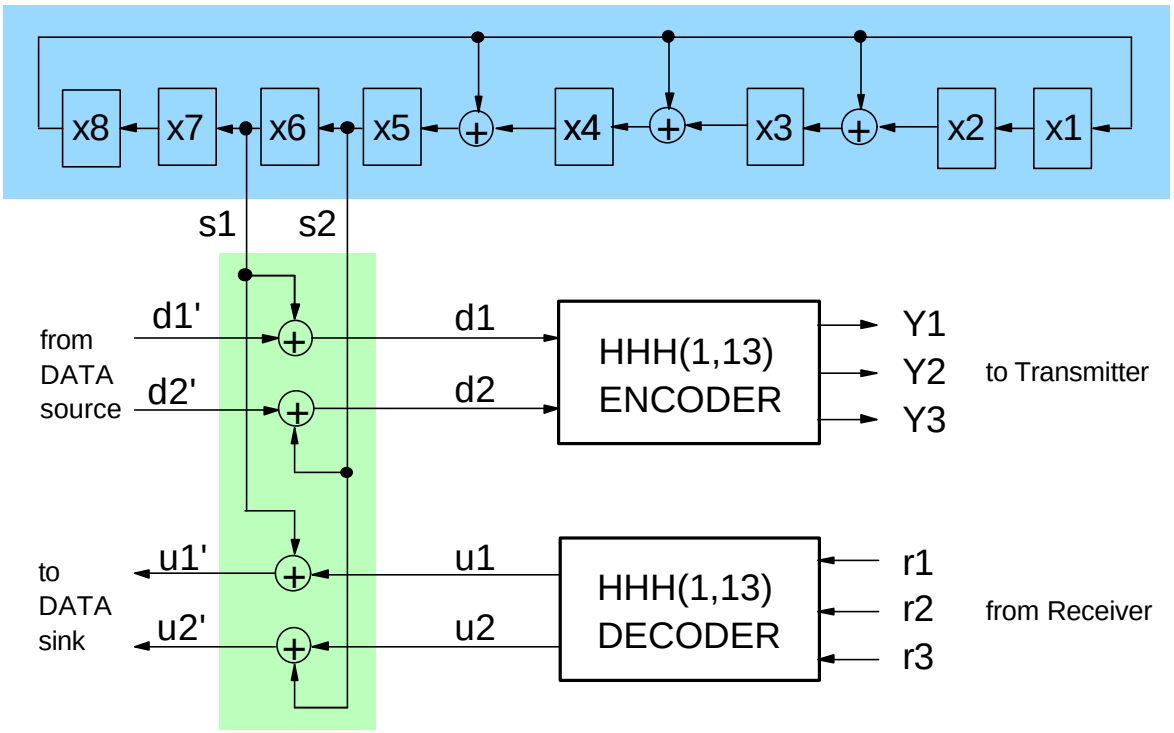


Fig 14. Reference Hardware to implement the scrambling/descrambling functions. The LFSR is implemented in the one-to-many form.

5.5.5 – State Table of Scrambler/Descrambler Reference Hardware

Table B1 represents the complete state table of the scrambler/descrambler hardware shown in Fig. B1 where we have defined that a new state is reached after the LFSR has been clocked *twice*. The LFSR's state is represented by its contents, i.e., (x8, x7, x6, x5, x4, x3, x2, x1), $x_i \chi$ [0, 1], …i. The table lists also the scrambling/descrambling bit pairs (s1, s2) = (x6, x5) that are valid in each state. The state sequence {(x8, x7, x6, x5, x4, x3, x2, x1)} and thus the sequence of scrambling/descrambling bit pairs {(s1, s2)} have period 255, i.e., they both repeat after 255 scrambling/descrambling cycles. The all-0 state (x8, x7, x6, x5, x4, x3, x2, x1) = (0, 0, 0, 0, 0, 0, 0, 0) does not occur (it is not allowed at any time). The table also indicates that the equivalent serial sequence formed from the pair sequence {(s1, s2)} consists of two periods of the maximum-length pseudo-random sequence (MLPRS) of length 255 bits, as determined by the scrambling/descrambling polynomial shown above.

5.5.5.1 Example of Scrambled/Descrambled Data Sequences:

The scrambled sequence, {(d1, d2)}, in this example corresponds to Example 1 in Section A5 of Appendix A.

Payload sequence:	{(d1', d2')}	= (0, 0) (0, 1) (0, 0) (1, 1) (1, 1) (1, 1) (0, 1) (0, 1)
Scrambling sequence:	{(s1, s2)}	= (1, 1) (0, 1) (0, 0) (1, 1) (0, 0) (1, 1) (0, 1) (0, 1)
Scrambled sequence:	{(d1, d2)}	= (1, 1) (0, 0) (0, 0) (0, 0) (1, 1) (0, 0) (0, 0) (0, 0)
Decoded scrambled sequence:	{(u1, u2)}	= (1, 1) (0, 0) (0, 0) (0, 0) (1, 1) (0, 0) (0, 0) (0, 0)
Descrambling sequence:	{(s1, s2)}	= (1, 1) (0, 1) (0, 0) (1, 1) (0, 0) (1, 1) (0, 1) (0, 1)
Descrambled payload sequence:	{(u1', u2')}	= (0, 0) (0, 1) (0, 0) (1, 1) (1, 1) (1, 1) (0, 1) (0, 1)

Legend:

a	= count index for scrambling/descrambling cycle
bcdefghi	= x8, x7, x6, x5, x4, x3, x2, x1 (LFSR contents = state)
jk	= s1, s2 (pair of scrambling/descrambling bits)

*) First cycle of the first scrambling/descrambling period (a = 1)

First bit of first serial MLPRS (a =1: j = s1 = x6)

↓

Second bit of first serial MLPRS (a = 1: k = s2 = x5)

↓

	a	bcdefghi	jk	a	bcdefghi	jk	a	bcdefghi	jk	a	bcdefghi	jk
*)	1	11111111	11	65	01000110	00	129	11100011	10	193	10001100	00
	2	11011011	01	66	00000101	00	130	10101011	10	194	00001010	00
	3	01001011	00	67	00010100	01	131	10010110	01	195	00101000	10
	4	00110001	11	68	01010000	01	132	01100010	10	196	10100000	10
	5	11000100	00	69	01011101	01	133	10010101	01	197	10111010	11
	6	00110111	11	70	01101001	10	134	01101110	10	198	11010010	01
	7	11011100	01	71	10111001	11	135	10100101	10	199	01101111	10
	8	01010111	01	72	11011110	01	136	10101110	10	200	10100001	10
	9	01000001	00	73	01011111	01	137	10000010	00	201	10111110	11
	10	00011001	01	74	01100001	10	138	00110010	11	202	11000010	00
	11	01100100	10	75	10011001	01	139	11001000	00	203	00101111	10
	12	10001101	00	76	01011110	01	140	00000111	00	204	10111100	11
	13	00001110	00	77	01100101	10	141	00011100	01	205	11001010	00
	14	00111000	11	78	10001001	00	142	01110000	11	206	00001111	00
	15	11100000	10	79	00011110	01	143	11011101	01	207	00111100	11
	16	10100111	10	80	01111000	11	144	01010011	01	208	11110000	11
	17	10100110	10	81	11111101	11	145	01010001	01	209	11100111	10
	18	10100010	10	82	11010011	01	146	01011001	01	210	10111011	11
	19	10110010	11	83	01101011	10	147	01111001	11	211	11010110	01
	20	11110010	11	84	10110001	11	148	11111001	11	212	01111111	11
	21	11101111	10	85	11111110	11	149	11000011	00	213	11100001	10
	22	10011011	01	86	11011111	01	150	00101011	10	214	10100011	10
	23	01010110	01	87	01011011	01	151	10101100	10	215	10110110	11
	24	01000101	00	88	01110001	11	152	10001010	00	216	11100010	10
	25	00001001	00	89	11011001	01	153	00010010	01	217	10101111	10
	26	00100100	10	90	01000011	00	154	01001000	00	218	10000110	00
	27	10010000	01	91	00010001	01	155	00111101	11	219	00100010	10
	28	01111010	11	92	01000100	00	156	11110100	11	220	10001000	00
	29	11110101	11	93	00001101	00	157	11110111	11	221	00011010	01
	30	11110011	11	94	00110100	11	158	11111011	11	222	01101000	10
	31	11101011	10	95	11010000	01	159	11001011	00	223	10111101	11
	32	10001011	00	96	01100111	10	160	00001011	00	224	11001110	00
	33	00010110	01	97	10000001	00	161	00101100	10	225	00011111	01
	34	01011000	01	98	00111110	11	162	10110000	11	226	01111100	11
	35	01111101	11	99	11111000	11	163	11111010	11	227	11101101	10
	36	11101001	10	100	11000111	00	164	11001111	00	228	10010011	01
	37	10000011	00	101	00111011	11	165	00011011	01	229	01110110	11
	38	00110110	11	102	11101100	10	166	01101100	10	230	11000101	00
	39	11011000	01	103	10010111	01	167	10101101	10	231	00110011	11
	40	01000111	00	104	01100110	10	168	10001110	00	232	11001100	00
	41	(next page)		105	(next page)		169	(next page)		233	(next page)	

(continued from previous page)

a	bcdefghi	jk	a	bcdefghi	jk	a	bcdefghi	jk	a	bcdefghi	jk	
41	00000001	00	105	10000101	00	169	00000010	00	233	00010111	01	
42	00000100	00	106	00101110	10	170	00001000	00	234	01011100	01	
43	00010000	01	107	10111000	11	171	00100000	10	235	01101101	10	
44	01000000	00	108	11011010	01	172	10000000	00	236	10101001	10	
45	00011101	01	109	01001111	00	173	00111010	11	237	10011110	01	
46	01110100	11	110	00100001	10	174	11101000	10	238	01000010	00	
47	11001101	00	111	10000100	00	175	10000111	00	239	00010101	01	
48	00010011	01	112	00101010	10	176	00100110	10	240	01010100	01	
49	01001100	00	113	10101000	10	177	10011000	01	241	01001101	00	
50	00101101	10	114	10011010	01	178	01011010	01	242	00101001	10	
51	10110100	11	115	01010010	01	179	01110101	11	243	10100100	10	
52	11101010	10	116	01010101	01	180	11001001	00	244	10101010	10	
53	10001111	00	117	01001001	00	181	00000011	00	245	10010010	01	
54	00000110	00	118	00111001	11	182	00001100	00	246	01110010	11	
55	00011000	01	119	11100100	10	183	00110000	11	247	11010101	01	
56	01100000	10	120	10110111	11	184	11000000	00	248	01110011	11	
57	10011101	01	121	11100110	10	185	00100111	10	249	11010001	01	
58	01001110	00	122	10111111	11	186	10011100	01	250	01100011	10	
59	00100101	10	123	11000110	00	187	01001010	00	251	10010001	01	
60	10010100	01	124	00111111	11	188	00110101	11	252	01111110	11	
61	01101010	10	125	11111100	11	189	11010100	01	253	11100101	10	
62	10110101	11	126	11010111	01	190	01110111	11	254	10110011	11	
63	11101110	10	127	01111011	11	191	11000001	00	255	11110110	11	^)
64	10011111	01	128	11110001	11	192	00100011	10	[256	11111111	11]	″)

↑
First bit of second serial MLPRS (a = 128: k = s2 = x5)

↑
Last (255th) bit of first serial MLPRS (a = 128: j = s1 = x6)

^) End of the first scrambling/descrambling period (a = 255)

″) Start of the second scrambling/descrambling period (a = 256 ≡ 1)

Table 17: The complete state table of the scrambler/descrambler reference hardware shown in Fig.14.

5.5.5 Aborted Packets

Receivers may only accept packets that have valid STA, IrLAP frame, CRC, and STO fields as defined in the Packet Format section. The PA field need not be valid in the received packet. All other packets are aborted and ignored.

5.5.6 Back to Back Packet Transmission

Back to back, or "brick-walled" packets are allowed, but each packet must be complete (i.e., containing PA, STA, IrLAP Frame, CRC and STO fields).

Appendix A. Test Methods

Note- A.1 is Normative unless otherwise noted. The rest of Appendix A and all of Appendix B are Informative, not Normative {i.e., it does not contain requirements, but is for information only}. Examples of measurement test circuits and calibration are provided in IrDA Serial Infrared Physical Layer Measurement Guidelines.

A.1. Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately.

1. Electromagnetic field: 3 V/m maximum
   Refer to IEC 61000-4-3 test level 2 for details.
   (For devices that intend to connect with or operate in the vicinity of a mobile phone or pager, a field of 30 V/m with frequency ranges from 800 Mhz to 960 Mhz and 1.4 GHz to 2.0 GHz including 80% amplitude modulation with a 1 kHz sine wave is recommended. Refer to IEC 61000-4-3 test level 4 for details. The 30 V/m condition is a recommendation; 3 V/m is the normative condition.)

2. Sunlight: 10 kilolux maximum at the optical port
   This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width less than 50 nm biased to provide 490 μW/cm^2 (with no modulation) at the optical port. The light source faces the optical port.

   This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radiation is covered by the incandescent condition.

3. Incandescent Lighting: 1000 lux maximum
   This is produced with general service, tungsten-filament, gas-filled, inside-frosted lamps in the 60 Watt to 150 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 degrees Kelvin range and a spectral peak in the 850 nm to 1050 nm range.

4. Fluorescent Lighting : 1000 lux maximum
   This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal (0 μW/cm^2 minimum and 0.3 μW/cm^2 peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz.

   Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.

A.2. Active Output Specifications

A.2.1. Peak Wavelength

The peak wavelength (Peak Wavelength, Up, um) is the wavelength of peak intensity and can be measured using an optical spectrum analyzer. The pulse shape and sequence can be the same as that used for the power measurements below and the measurement can be made on the optical axis.

A.2.2. Intensity and Angle

The following three specifications form a set that can be measured concurrently:

- Maximum Intensity In Angular Range, mW/sr
- Minimum Intensity In Angular Range, mW/sr
- Half-Angle, degrees

This intensity measurement requires means to measure optical power as well as the distance and angle from a reference point. Power measured in milliwatts (mW) or microwatts (μW) is converted to intensity in mW/sr (or μW/sr) or irradiance in mW/cm^2 (or μW/cm^2). In addition, if there are any cosmetic windows or filters that are part of the interface, they must be in place for all intensity and spatial distribution optical measurements

The primary reference point is the center point of the surface of the IrDA optical port and the port's optical axis is the line through the reference point and normal to the port surface. Link specifications are based on the assumption that the maximum intensity at the port surface is 500 mW/cm^2 due to a point source of 500 mW/sr maximum intensity placed one centimeter behind the reference surface. Distance is measured radially from the reference point to the test head. Half-Angle is the angular deviation from the optical axis as shown in Figure 4. The plane of the detector at the Test Head is normal to the radial vector from the center of the optical port to the detector.

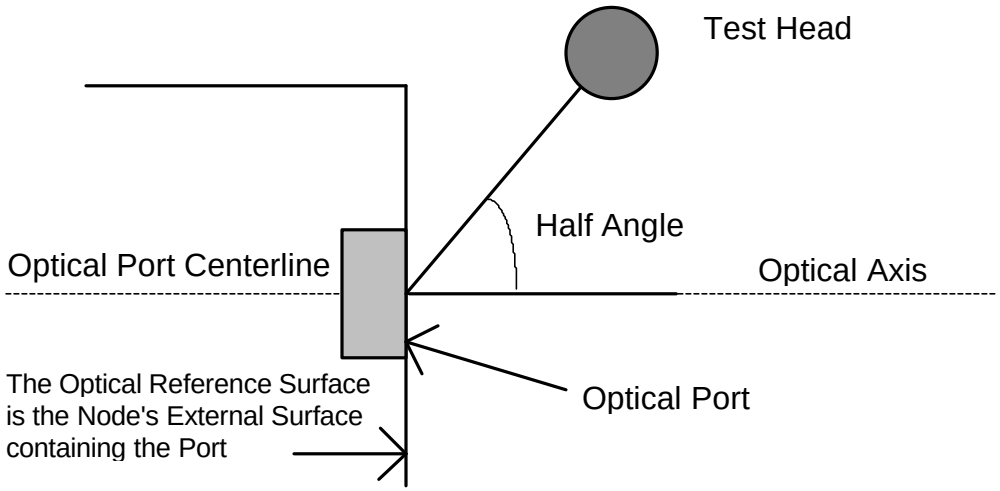


Figure 4. Optical Port Angle Measurement Geometry

The IrDA link specification is based on peak optical power levels. Power measurement can be made on a single pulse or by averaging a sequence of pulses and converting to peak levels. Averaging methods require knowledge of the pulse sequence and/or duty factor in order to calculate the peak power from the reported average. In addition, for short pulse durations, attention must be paid to the effect of the rise and fall times of the optical signal on the effective optical pulse duration.

The test head is to be calibrated to provide accurate results for signals within the appropriate ranges of wavelength, pulse and pulse sequence characteristics. The size of the photodetector in the test head must be known in order to translate the results from power (mW or μW) to irradiance (mW/cm^2 or μW/cm^2) and intensity (mW/sr or μW/sr). Finally, the test head should be aimed directly at the reference point, i.e., the test detector should be normal to the vector from the center of the optical port to the center of the test detector.

The power measurement should be made at a distance large enough to avoid near field optical effects but close enough to receive a robust signal. To test for an appropriate distance, make power measurements at half and double the chosen distance and check that the results are consistent with an inverse square relationship.

Resolution of spatial intensity variation should be as fine as the smallest detector. Unfortunately, because the detected signal intensity is averaged over the size of the test head, resolution becomes a tradeoff with signal strength. However, there is no size constraint in the Active Input Interface specification for the detector in the IrDA receiver. It is impractical to test with an infinitesimal detector. A suggested test setup employs a 1 cm^2 area photodiode at a distance of 30 cm from the emitter. For a circular photodiode, the

diameter is 1.13 mm, which subtends an angle of 1.08°, or 0.00111 steradians. Any measurement setup should have at least this angular resolution.

Figure 5 contains a graphical representation of the serial infrared Active Output Interface specifications. The measured intensity must be less than or equal to "Maximum Intensity In Angular Range" in the angular region less than or equal to 30 degrees and less than or equal to "Minimum Intensity In Angular Range" in the angular region greater than 30 degrees. The measured intensity must be greater than or equal to "Minimum Intensity In Angular Range" in the angular region less than or equal to 15 degrees. The minimum allowable intensity value is indicated by “min” in Figure 5, since the actual specified value is dependent upon data rate.

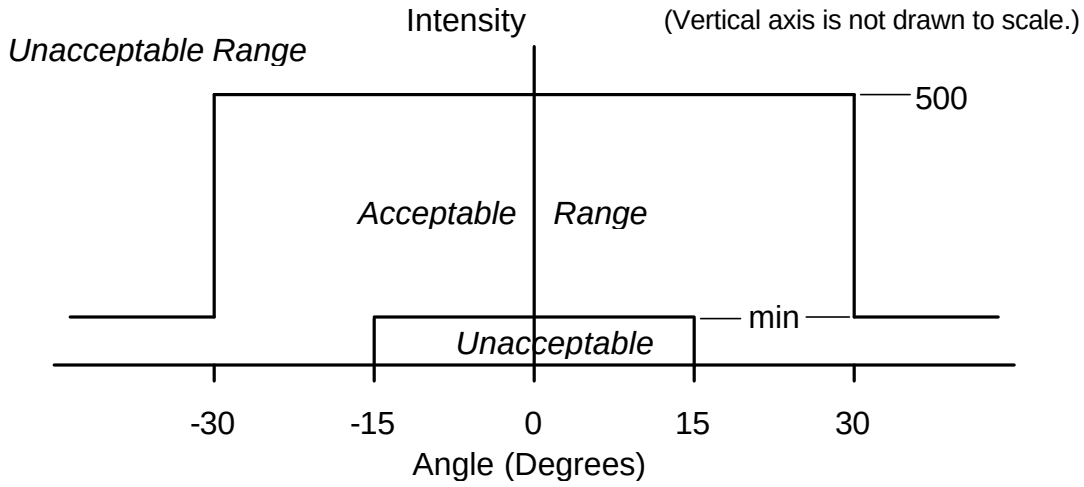


Figure 5. Acceptable Optical Output Intensity Range

The optical power measurements are converted to optical intensity across the +/- 30 degree region to verify both the maximum and minimum intensity specifications and sufficiently beyond +/- 30 degrees to verify the specification. Optical power is converted to intensity by the relationship

Intensity(mW/sr) = [Power(mW)]/[Detector Solid Angle(sr)].

The Detector Solid Angle in steradians is given by the relationship

Detector Solid Angle (sr) = 2pi[1-cos(Half-Angle)],

where the Half-Angle is half the angle subtended by the detector, viewed from the reference point.

The Detector Solid Angle can be approximated with the relationship

Detector Solid Angle (sr) ~ [Area of Detector]/[r^2],

where r is the distance between the test head and the reference point.

A.2.3. Pulse Parameters and Signaling Rate

The following six specifications form a set that can be measured with the same set-up:

- Rise Time tr, 10-90%, µs or ns
- Fall Time tf, 90-10%, µs or ns
- Pulse Duration, % of Bit or Symbol Period
- Optical Over Shoot, %
- Edge Jitter, µs or ns
- Signaling Rate, kbit/s or Mbit/s

These measurements require means to measure optical power and an oscilloscope (or equivalent) with sufficient bandwidth to resolve jitter to better than 0.2 μs (for data rates up to and including 115.2 kbit/s). For the data rates up to 4.0 Mbit/s, jitter down to 10 ns must be resolved. For 16.0 Mbit/s, the jitter is about 3 ns. Thus, the oscilloscope bandwidth should be sufficiently high to observe the jitter.

Definitions of the reference point, etc., are the same as for the Active Output Interface power measurements and the same considerations for test distance and signal strength apply. The test head should be positioned within +/-15 degrees of the optical axis and aimed directly at the reference point.

Rise Time, Fall Time, Pulse Duration and Overshoot can be measured for a single optical pulse. Since overshoot is referenced to the pulse amplitude at the end of the pulse, the maximum duration pulses should be used in this test. For Rise Time, Fall Time, Pulse Duration and Overshoot, refer to Figure 6. It is critical to determine the 100% level, since all four of these parameters are dependent upon it. If there is uncertainty concerning the existence of the flat region that defines the 100% level (is there over shoot, or does the pulse have a long, rounded top?), measurements at a longer drive pulse duration will resolve this, and allow easier determination of the 100% level.

Jitter and Signaling Rate require a sequence of pulses for determination. For data rates up to and including 115.2 kbit/s, the signal is asynchronous at the byte; therefore Jitter and Signal Rate are only relevant within a byte. For 0.576 Mbit/s, 1.152 Mbit/s and 4.0 Mbit/s, however, the optical bit stream is synchronous for up to 500 ms, though typically less than 20 ms (window = 7, packet size = 2k). Thus, the measurement requires the accumulation of data over a longer time interval.

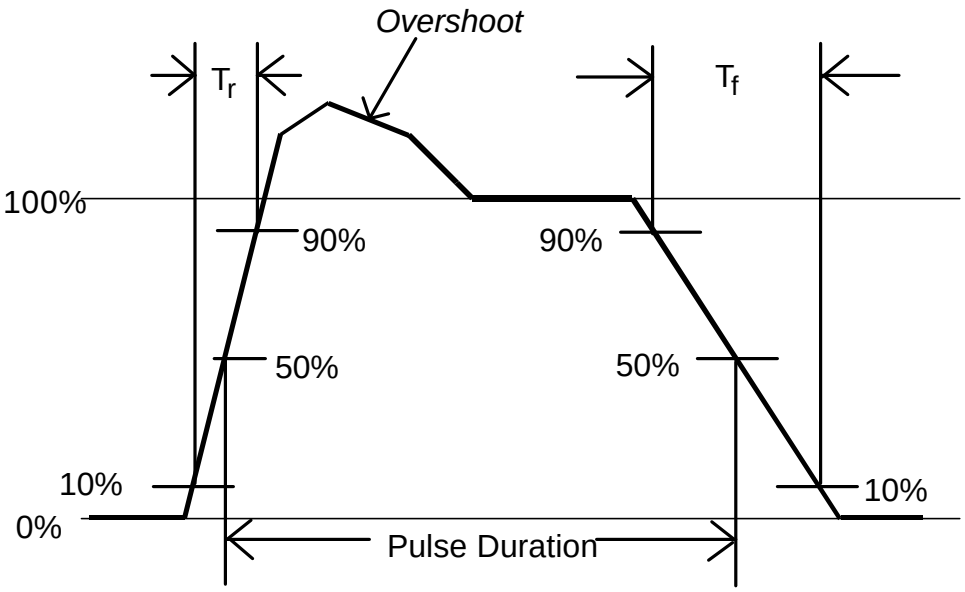


Figure 6. Pulse Parameter Definitions

The reciprocal of the mean of the absolute delay times between optical pulses is the data rate. Although some accuracy should be gained by the averaging, for only 1 asynchronous byte the tolerance requirement may be difficult to achieve with an oscilloscope. If UART frames are back to back (synchronous across bytes), use of an oscilloscope may be adequate. If access to an internal clock signal is available, a counter may be used.

For rates up to and including 115.2 kbit/s, we can consider jitter to be the range of deviation between the leading edge of the optical pulse and a reference signal edge. Refer to Figure 7. For simplicity, the reference signal can be taken to be the leading edge of the first pulse in the byte (the “Start” pulse). Using the nominal data rate, the arrival time of each pulse in the byte can be predicted. The jitter (in time units) is

the maximum departure from predicted arrival time of the actual arrival time. Since jitter may be pattern dependent, various data should be used in the test signal.

For 0.576 Mbit/s and 1.152 Mbit/s RZI and 4.0 Mbit/s 4PPM and 16.0 Mbit/s HHH(1,13), an entire packet can be used to determine jitter. The optical signal should be detected using a high speed optical detector (e.g., a reverse-biased, small silicon p-i-n diode). The detector output signal is displayed using a storage oscilloscope set to trigger as often as possible during a packet, the stored image displaying an eye diagram. Care should be taken to use time constants in any ac coupling which are much, much longer than the symbol times.. The jitter (in time units) is half of the horizontal “smear” of the eye signal at the 50% level, where the leading and trailing edges of the signal cross (see Figure 8). To determine data rate, a counter may be used at 4.0 Mbit/s and 16.0 Mbit/s if a sufficiently long data transmission is available. For 0.576 Mbit/s and 1.152 Mbit/s, an oscilloscope and back to back packets are recommended to determine data rate.

For 0.576 and 1.152 Mbit/s, there may be some implementations which use a digital synthesizer to generate the transmitter clock. In this case, there may be jitter of up to +/- 25 ns relative to an idealized reference clock. Typically, with a 40 MHz primary clock, the jitter would be +/- 12.5 ns from the synthesizer, and another 5 ns or so from the driver and LED.

The jitter may be measured indirectly by using a high speed photodiode and a digitizing oscilloscope to measure the variance in edge to edge delay. Configure the transmitter to repetitively send large (2kb) packets of data (approximately 2 ms), and trigger the oscilloscope on any rising optical edge. Capture a section of the waveform delayed from the reference edge by 1 to 31 times the bit period. Capture several hundred repetitions at each delay, and measure the spread in the edge locations. It is necessary to measure at several delays since any one delay might be a multiple of the clock synthesis cycle, and show artificially small jitter. Measurements at several prime intervals should be sufficient, e.g., at 3, 7, 13 ,19, and 31 times the bit period. The jitter relative to a "reference" clock is one half of the worst case spread in the rising edges at each delay.

The jitter may also be measured relative to a reference clock generated with an analog phase locked loop with a tracking bandwidth of about 10 kHz, locked to the optical signal edges. In this case, the oscilloscope should be triggered on the reference clock edge, and several hundred optical signal edges should be collected. Adequate time must be allowed for the PLL to settle before collecting edges, so the oscilloscope trigger should be gated for several PLL time constants after the beginning of a packet.

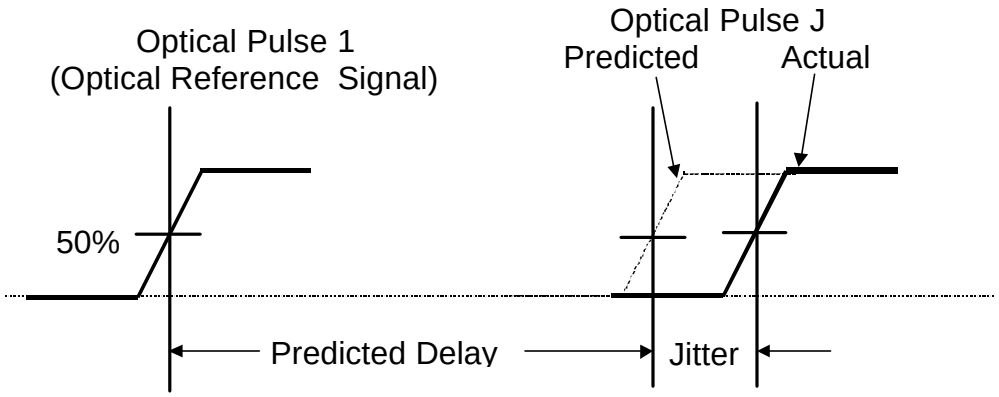


Figure 7. Pulse Delay and Jitter Definitions

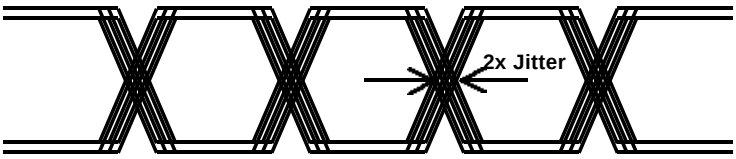


Figure 8. 4.0 Mbit/s Jitter Definitions

A.2.4. Eye Safety Standard

The apparent source size is a parameter used in determining the power or energy Accessible Emission Level Class limits and the measurement conditions of IEC 60825-1 and CENELEC EN60825-1.

The apparent source size is how large the source appears (how tightly the power or energy is concentrated). One method to determine apparent source size is to form an image of the source with a relay lens, as shown in Figure 9. By placing the emitter at a distance of twice the focal length of the lens, an image of size equal to the source will form at the same distance on the other side of the lens. The image can then be scanned with a small photodiode to determine the distribution of emitted light. Alternatively, a CCD camera system can be used; several of these systems on the market include software for analyzing the image.

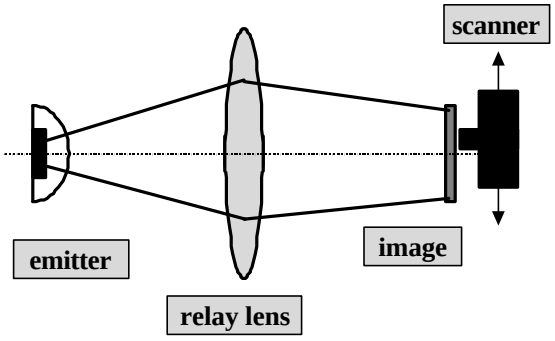


Figure 9. Apparent Source Size Measurement

The apparent source size, s, is deemed to be the diameter of the smallest circular aperture containing approximately 63.2% of the incident light.

Measurements of source output power must be made at the correct distance, r, and with the correct aperture diameter, d. Under the amendment to IEC 60825-1 (and CENELEC EN60825-1) the measurement conditions for measuring output power, source to measurement aperture distance, r, and aperture diameter, d, are functions of apparent source size, s in mm or α (mrad). The eye safety standard used angles for defining source sizes. When using a fixed distance of 100mm, source size and apparent angular source size can be calculated simply by s (mm) = α (mrad)/10. The constants αmin and αmax are given with α_{min} = 1.5 mrad and α_{max} = 100mrad.

The measurement distance, r, measurement aperture diameter, d, are derived from apparent source size, s, as follows:

Aperture Diameter (d)	Measurement Distance (r)

Fixed 7.0 mm aperture in 14 mm to 100 mm distance r	$r = (100mm) \times \sqrt{\frac{a + 0.46mrad}{a_{\max}}}$ if $\alpha < \alpha_{min,}$ r = 14 mm. If $\alpha \geq \alpha_{max}$, r = 100 mm
$d = (7mm) \times \sqrt{\frac{a_{\max}}{a + 0.46mrad}}$ if $\alpha < \alpha_{min,}$ d = 50 mm. If $\alpha \geq \alpha_{max}$, d = 7 mm	Variable 7 – 50 mm aperture d in 100 mm distance

Table 5. Measurement Parameters

These relationships apply for s between 0.15 mm and 10 mm, which probably includes all IrDA compliant emitters.

A fixed aperture of 7.0 mm can be easier to implement, and then adjust the measurement distance according to the calculation. Whether the aperture is fixed at 7.0 mm or the distance is fixed at 100 mm, only light output power passing through the aperture is measured for comparison to the AEL Class limits.

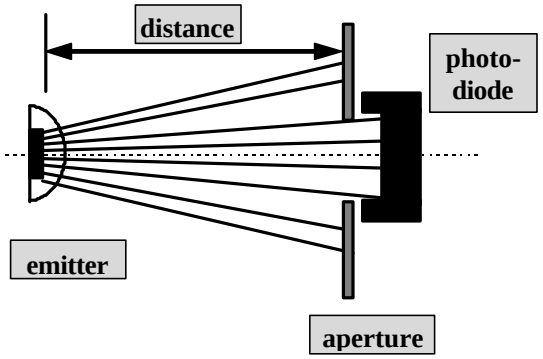


Figure 10. IEC 60825-1 AEL Classification Power Measurement

Source output power can be derived from measured photocurrent resulting from light collected on a calibrated photodiode detector. Measured photocurrent in amps can be converted to detected power in watts, using the calibration factor in A/W (amps/watt).

For source wavelength λ = 700-1050 nm, the AEL Class 1 limit is calculated as:

Parameters: IREDs 700 nm to 1050 nm, relevant time base, CW or averaged operation, thermal limits

Timebase [s] Conditions	60825-1 Amendment 2 (Jan. 2001)
Timebase = 100 s, $\alpha \leq 1.5$ mrad, $t > T_2$	$7 \times 10^{-4} C_4 C_7$ W
Timebase = 100 s, $\alpha > 1.5$ mrad, $t > T_2$	$7 \times 10^{-4} C_4 C_6 C_7 T_2^{-0.25}$ W
Timebase = 100 s $t \leq T_2$	$7 \times 10^{-4} t^{0.75} C_4 C_6 C_7$ J
Constants	
C_4	$C_4 = 10^{0.02(\lambda - 700)}$

C_6	$C_6 = 1, \alpha \le \alpha_{min}$
C_6	$C_6 = \alpha/\alpha_{min}, \alpha_{min} < \alpha < \alpha_{max}$
C_6	$C_6 = \alpha_{max}/\alpha_{min} = 66.7, \alpha > \alpha_{max}$
C_7	$C_7 = 1$
T_2	$T_2 = 10 \times 10^{\left[\frac{(\alpha - \alpha_{min})}{98.5}\right]}$ s
α_{min}	α_{min} = 1.5 mrad α_{max} = 100 mrad

Table 5a: Accessible emission limits for class 1 (and class 1M) laser products

The recent modification (effective January 2001) changes the minimum source angular subtense (1.5mrad as against 11mrad) and adds two break points for the exposure time t(T1 and T2). In case of IrDA transmission, the break point T2 is 10 s for α <1.5 mrad and 100s for α > 100 mrad.

For other cases, T2 is computed as given with the relation in the table above.

The relation between angular subtense α and apparent source size diameter s is given by
α = 1000 x [2 x $\tan^{-1}$((s/2)/100 mm] (mrad)
s = apparent source size (mm)

The AEL Class 1 limit can be calculated by the formula given in the table above.

It is convenient to express both the AEL Class limit and the measured AEL of the system in terms of W/sr (watts/steradian). System source radiant intensity is often specified in mW/sr (milliwatts per steradian).

Apparent source angular subtense, α, is the 2-dimensional angle subtended by the source's radiated light image at a distance of 100 mm. A 3-dimensional angle (solid angle) subtended by the source's radiated light image can be expressed in units of steradians. A hemisphere (1/2 of a sphere) subtends a solid angle of 2π steradians. The solid angle, Ω, subtended by a cone of full angle, θ, is given by:

$$\Omega = 2\pi (1 - \cos(\theta/2))$$

Given the measurement distance, r, and the aperture diameter, d, the solid angle given by:

$$\Omega = 2\pi (1 - \cos(\tan^{-1}(d/2r)))$$

The measured AEL and AEL Class limits can now be expressed in watts/steradian:

AEL (watts/steradian) = AEL (watts) / Ω (steradians)

Given the measurement distance, r, and the aperture diameter, d, the AEL is:

AEL (mW/sr) = AEL (mW)/ (2π (1 - cos($\tan^{-1}$(d/2r))))

Once the source radiant intensity in milliwatts/steradian has been determined, it can be compared with the AEL Class limits for classification. If the output does not exceed the Class 1 limit, the operation is Class 1. For more information, refer to IEC 60825-1 or CENELEC EN 60825-1 and their amendments.

A.3. Active Input Specifications

The following five specifications form a set which can be measured concurrently:

- Maximum Irradiance in Angular Range, mW/cm^2
- Minimum Irradiance in Angular Range, µW/cm^2
- Half-Angle, degrees
- Bit Error Ratio, (BER)
- Receiver Latency Allowance, ms

These measurements require an optical power source and means to measure angles and BERs. Since the optical power source must provide the specified characteristics of the Active Output, calibration and control of this source can use the same equipment as that required to measure the intensity and timing

characteristics. BER measurements require some method to determine errors in the received and decoded signal. The latency test requires exercise of the node's transmitter to condition the receiver.

Definitions of the reference point, etc., are the same as for the Active Output Interface optical power measurements except that the test head is now an optical power source with the in-band characteristics (Peak Wavelength, Rise and Fall Times, Pulse Duration, Signaling Rate and Jitter) of the Active Output Interface. The optical power source also must be able to provide the maximum power levels listed in the Active Output Specifications. It is expected that the minimum levels can be attained by appropriately spacing the optical source from the reference point.

Figure 11 illustrates the region over which the Optical High State is defined. The receiver is operated throughout this region and BER measurements are made to verify the maximum and minimum requirements. The ambient conditions of A.1 apply during BER tests; BER measurements can be done with worst case signal patterns. Unless otherwise known, the test signal pattern should include maximum length sequences of "1"s (no light) to test noise and ambient, and maximum length sequences of "0"s (light) to test for latency and other overload conditions.

The minimum allowable intensity value is indicated by “minimum” in Figure 11, since the actual specified value is dependent upon data rate.

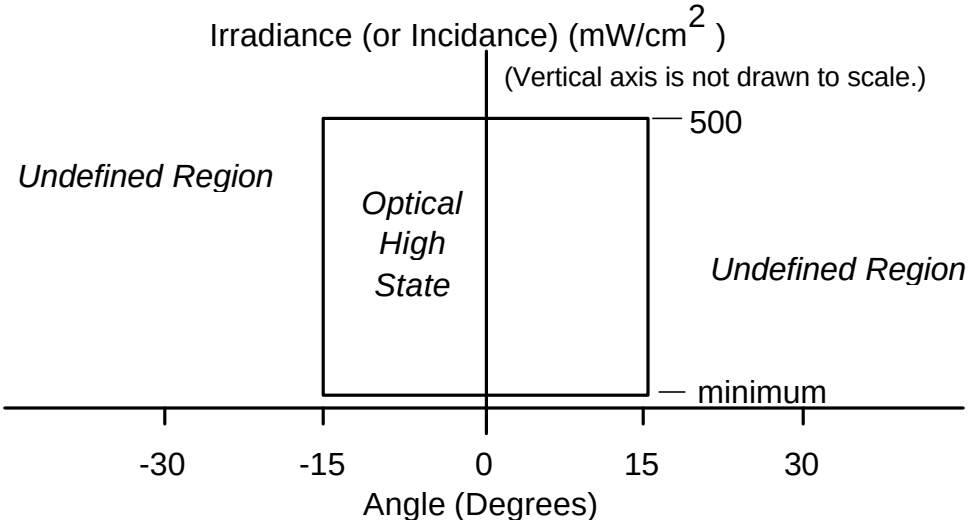


Figure 11. Optical High State Acceptable Range

Latency is tested at the Minimum Irradiance in Angular Range conditions. The receiver is conditioned by the exercise of its associated transmitter. For rates up to and including 1.152 Mbit/s, the conditioning signal should include maximum length sequences of "0"s (light) permitted for this equipment. For 4.0 Mbit/s 4PPM operation, various data strings should be used; the latency may be pattern dependent. The receiver is operated with the minimum irradiance levels and BER measurements are made after the specified latency period for this equipment to verify irradiance, half-angle, BER and latency requirements.

Appendix B. An Example of One End of a Link Implementation

Appendix B is Informative, not Normative {i.e., it does not contain requirements, but is for information only}. Specifications in Table 6 are derived from tables earlier in the document.

The link implementations in this appendix are examples only. All links must operate at 9.6 kbit/s. Specifications are used as constraints, but all other parameters' values are calculated for the purpose of providing a more complete example.

B.1. Definitions

UART - Universal Asynchronous Receiver/Transmitter: an electronic device/module that interfaces with a serial data channel.

B.2. Physical Representations

A block diagram of one end of an overall serial infrared link for data rates up to and including 115.2 kbit/s is shown in Figure 12a. Figure 12b shows on overall configuration for a link supporting the lower speeds as well as 0.576 Mbit/s, 1.152 Mbit/s and 4.0 Mbit/s.

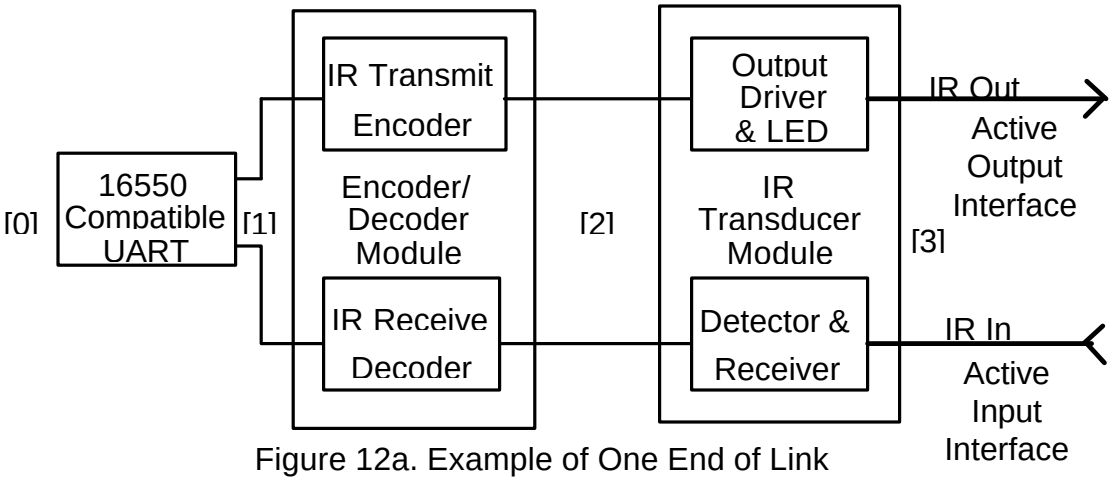


Figure 12a. Example of One End of Link
For Signaling Rates Up to & Including 115.2 kb/s

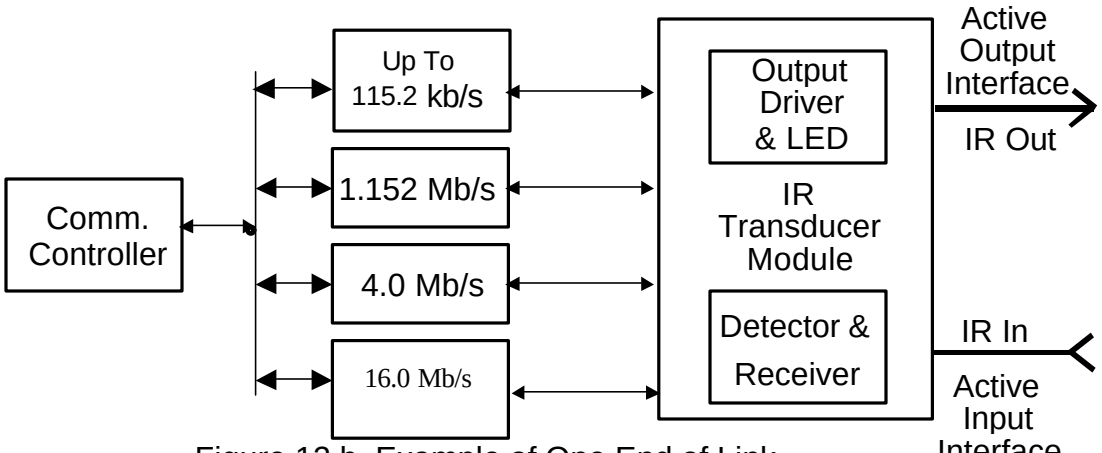


Figure 12 b. Example of One End of Link
For Signaling Rates Up to 16.0 Mb/s

B.3. Functionality & Electrical Waveforms - Data Rates Up to & Including 115.2 kbit/s

In Figure 12a, the signal to the left of the UART [0] will not be discussed. The signal between the UART and the Encoder/Decoder [1] is a bit stream of pulses in a frame comprised a Start Bit, 8 Data Bits, no Parity Bit and ending with a Stop Bit, as shown in Figure 13a.

The signal at [2], between the Encoder/Decoder Module and the IR Transducer Module is shown in Figure 13b. The electrical pulses between the IR Transmit Encoder and the Output Driver & LED are 3/16 of a bit period in duration (or, for the slower signaling rates, as short as 3/16 of the bit period for 115.2 kbit/s). Note that the IR Transmit Encoder and the Output Driver and LED pulses begin at the center of the bit period. The electrical pulses between the Detector & Receiver and the IR Receive Decoder are nominally of the same duration as those between the IR Transmit Encoder and the Output Driver & LED, but may be longer in some implementations. Thus, the electrical signals at [2] are analogs of the optical signals at [3]; an example of a nominal waveform is shown in Figure 13b. A "0" is represented by a pulse and a "1" is represented by no pulse.

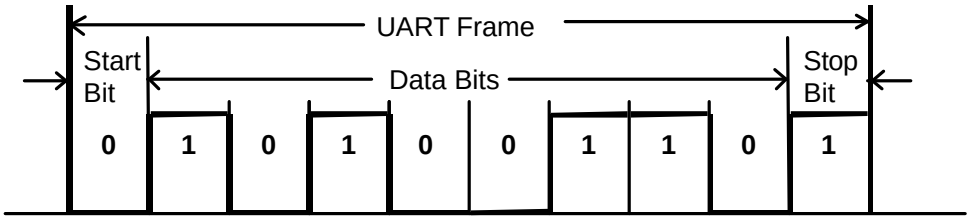


Figure 13a. UART Frame

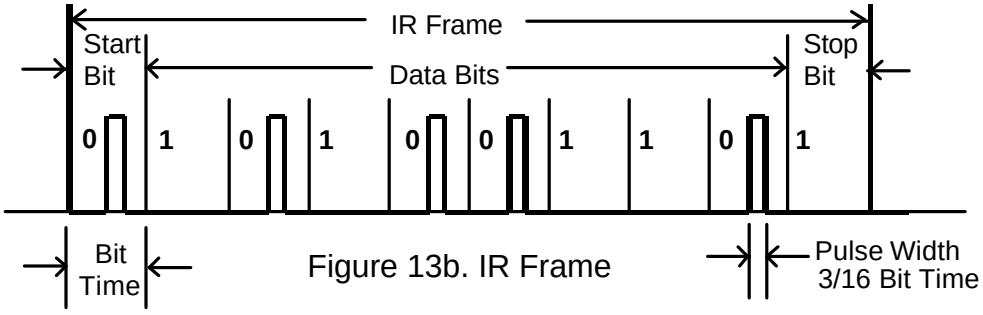


Figure 13b. IR Frame

B.4. Receiver Data and Calculated Performance

Examples in this section are provided to show receiver implementations which are sufficient to meet the BER requirements called for in section 4 for minimum irradiance conditions. The highest signaling rate for each of the encoding formats is used due to the bandwidth and noise consequences. The sunlight ambient is also used for its noise impact.

Photodiode currents are calculated for the minimum signal and sunlight conditions. Different effective optically receptive areas are assumed for the standard and low power options. Noise and eye loss calculations are based on an assumed high input impedance preamplifier model with a single high frequency pole and a single low frequency pole forming a bandpass filter where the only noise sources are thermal noise due to the input impedance and shot noise due to sunlight generated photodiode current. The high frequency pole is set by the impedance and capacitance at the input of the preamplifier.

Preamplifier output rise time (Channel Response Time) is calculated combining preamplifier and Active Output characteristics. Eye loss due to minimum pulse width and channel response time limiting the amplitude to less than 100% of pulse magnitude is calculated. Eye loss due to jitter is not calculated and margin is provided for this and other considerations.

The three segments of Table 6 appear in specifications in section 4 of the main body of this document and are repeated here for convenient reference. Tables 7, 8 and 9 present examples of 115.2 kbit/s receiver implementations for standard, low power and mixed operation. Tables 10, 11 and 12 present similar examples for 1.152 Mbit/s implementations as do Tables 13, 14 and 15 for 4.0 Mbit/s operation. Tables 7 through 15 also repeat specifications for convenient reference.

TERMS:

Detector Responsivity ($\mu A/(mW/cm^2)$) is a photodiode characteristic combining sensitivity (A/W) and effective area.

Channel Response Time is the 10% to 90% rise time produced by the rms combination of the Active Output rise time and step response rise time of the preamplifier.

Receiver Noise Current is the thermal noise associated with the impedance at the input of the preamplifier and the associated bandwidth.

Sunlight Ambient Noise Current is the shot noise associated with the sunlight induced photodiode current and the associated bandwidth.

Receiver Noise Current is the rms combination of the receiver and sunlight ambient noise currents.

Comparator Threshold is assumed to be at 50% of the minimum signal condition to yield optimum signal to noise ratios for both high and low states.

Specified Signal/Noise ratio for BER is the SNR calculated to achieve the required BER for a static signal level where the threshold is at 50% of the high state and noise is gaussian.

Receiver Margin is the ratio of the actual SNR to the Specified SNR for BER expressed in dB(optical).

Penalty: Eye Loss for Bandwidth Limits is the additional signal required for the minimum pulse width to reach 100% of the eye opening height expressed in dB(optical).

Margin for Edge Jitter, EMI, other is the signal margin above the Specified SNR for BER remaining after accounting for Eye Loss for Bandwidth Limits expressed in dB(optical).

LINK INTERFACE SPECIFICATIONS	Data Rates	Type	Minimum	Maximum
Signaling Rate	All	Both	See Table 2	See Table 2
Link Distance Lower Limit, m	All	Both	-	0
Minimum Link Distance Upper Limit, m	See Table 1	Both	See Table 1	-
Ambient Sunlight Irradiance**, μW/cm^2		Both	-	490
Bit Error Ratio, BER	All	Both		10^-8
ACTIVE OUTPUT SPECIFICATIONS				
Peak Wavelength, Up, μm	All	Both	0.85	0.90
Maximum Intensity In Angular Range, mW/sr	All	Std	-	500*
" " " " " "		LowPwr	-	72*
Minimum Intensity In Angular Range, mW/sr	≤ 115.2 kbit/s	Std	40	-
" " " " " "	≤ 115.2 kbit/s	LowPwr	3.6	-
" " " " " "	> 115.2 kbit/s	Std	100	-
" " " " " "	> 115.2 kbit/s	LowPwr	9	-
Half-Angle, degrees	All	Both	15	30
Rise Time tr, 10-90%, Fall Time Tf, 90-10% , ns	≤ 115.2 kbit/s	Both	-	600
Rise Time tr, 10-90%, Fall Time Tf, 90-10% , ns	> 115.2 kbit/s	Both	-	40
Rise Time tr, 10-90%, Fall Time Tf, 90-10% , ns	16 Mbit/s	Std	-	19
Pulse Duration	All	Both	See Table 2	See Table 2
Edge Jitter, % of nominal pulse duration	≤ 115.2 kbit/s	Both	-	+/-6.5
Edge Jitter Relative to Reference Clock, % of nominal bit duration	0.576 Mbit/s & 1.152 Mbit/s	Both	-	+/-2.9
Edge Jitter, % of nominal chip duration	4.0 Mbit/s	Both	-	+/-4.0
Edge Jitter, % of nominal chip duration	16.0 Mbit/s	Both	-	+/-4.0
ACTIVE INPUT SPECIFICATIONS				
Maximum Irradiance in Angular Range,mW/cm^2	All	Both	-	500
Minimum Irradiance In Angular Range, μW/cm^2	≤ 115.2 kbit/s	LowPwr	9.0	-
" " " " " "	≤ 115.2 kbit/s	Std	4.0	-
" " " " " "	> 115.2 kbit/s	LowPwr	22.5	-
" " " " " "	> 115.2 kbit/s	Std	10.0	-
Half-Angle, degrees	All	Both	15	-
Receiver Latency Allowance, ms	All	Std	-	10
" " " "	All	LP	-	0.5
Receiver Latency Allowance, ms	16.0 Mbit/s	Both	-	0.1

* For a given transmitter implementation, the IEC 60825-1 AEL Class 1 limit may be less than this. See section 2.4 above and Appendix A.

** Used for an example of ambient conditions. Allowance must be made for fluorescent and incandescent radiation as well as EMI.

Table 6. Serial Infrared Specifications for data rates up to 16.0 Mbit/s

B.4.1. 115.2 kbit/s Standard Implementation Example

(Standard transmitter to standard receiver for 115.2 kbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Signal Pulse Rate, kbit/s	114.2	116.2
Minimum Link Distance Upper Limit, m	1.0	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	4.0	
Min. Eff. Receiver Signal Detected Current, nA	175.8	-
Sunlight In-Band Photocurrent, A	2.15E-05	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.0015	
Receiver Upper 3 dB Bandwidth Limit, MHz		0.250
Receiver Input Noise Current, A	3.95E-10	-
Receiver Input Noise Current, A/(Hz)^0.5	7.93E-13	-
Sunlight Ambient Noise Current, A	1.64E-09	-
Total Receiver Input rms Noise Current, A	1.69E-09	-
Comparator Threshold = 0.5(Signal), nA	87.9	-
Receiver Signal Detected/Input Noise Current	104.2	-
Specified Signal/Noise Ratio For BER	11.2	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	9.68	-
Single Bit Pulse Width, Tb, ns	1410	-
Channel Response Time, Tc, ns	-	1523
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.93
Margin for Edge Jitter, EMI, other, dB	8.8	-

Table 7. Receiver Data and Calculated Performance for Standard Operation at 115.2 kbit/s

B.4.2. 115.2 kbit/s Low Power Option Implementation Example

(Low power transmitter to low power receiver for 115.2 kbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Signal Pulse Rate, kbit/s	114.2	116.2
Minimum Link Distance Upper Limit, m	0.20	
Detector Responsivity, µA/(mW/cm^2)	17.2	
Minimum Irradiance In Angular Range, µW/cm^2	9.0	
Min. Eff. Receiver Signal Detected Current, nA	154.5	-
Sunlight In-Band Photocurrent, A	8.41E-06	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.0015	
Receiver Upper 3 dB Bandwidth Limit, MHz		0.250
Receiver Input Noise Current, A	2.44E-10	-
Receiver Input Noise Current, A/(Hz)^0.5	4.89E-13	-
Sunlight Ambient Noise Current, A	1.02E-09	-
Total Receiver Input rms Noise Current, A	1.05E-09	-
Comparator Threshold = 0.5(Signal), nA	77.2	-
Receiver Signal Detected/Input Noise Current	146.6	-
Specified Signal/Noise Ratio For BER	11.2	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	11.17	-
Single Bit Pulse Width, Tb, ns	1410	-
Channel Response Time, Tc, ns	-	1523
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.93
Margin for Edge Jitter, EMI, other, dB	10.2	-

Table 8. Receiver Data and Calculated Performance for Low Power Operation at 115.2 kbit/s

B.4.3. 115.2 kbit/s Low Power Option/Standard Implementation Example

(Low power transmitter to standard receiver for 115.2 kbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Signal Pulse Rate, kbit/s	114.2	116.2
Minimum Link Distance Upper Limit, m	0.30	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	4.0	
Min. Eff. Receiver Signal Detected Current, nA	175.8	-
Sunlight In-Band Photocurrent, A	2.15E-05	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.0015	
Receiver Upper 3 dB Bandwidth Limit, MHz		0.250
Receiver Input Noise Current, A	3.95E-10	-
Receiver Input Noise Current, A/(Hz)^0.5	7.93E-13	-
Sunlight Ambient Noise Current, A	1.64E-09	-
Total Receiver Input rms Noise Current, A	1.69E-09	-
Comparator Threshold = 0.5(Signal), nA	87.9	-
Receiver Signal Detected/Input Noise Current	104.2	-
Specified Signal/Noise Ratio For BER	11.2	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	9.68	-
Single Bit Pulse Width, Tb, ns	1410	-
Channel Response Time, Tc, ns	-	1523
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.93
Margin for Edge Jitter, EMI, other, dB	8.8	-

Table 9. Receiver Data and Calculated Performance for Standard Receiver & Low Power Transmitter Operation at 115.2 kbit/s

B.4.4. 1.152 Mbit/s Standard Implementation Example

(Standard transmitter to standard receiver for 1.152 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Signal Pulse Rate, Mbit/s	1.1508	1.1532
Minimum Link Distance Upper Limit, m	1.0	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	10.0	
Min. Eff. Receiver Signal Detected Current, nA	439.4	-
Sunlight In-Band Photocurrent, A	2.15E-05	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.0151	
Receiver Upper 3 dB Bandwidth Limit, MHz		2.48
Receiver Input Noise Current, A	3.92E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	2.50E-12	-
Sunlight Ambient Noise Current, A	5.17E-09	-
Total Receiver Input rms Noise Current, A	6.49E-09	-
Comparator Threshold = 0.5(Signal), nA	219.7	-
Receiver Signal Detected/Input Noise Current	67.8	-
Specified Signal/Noise Ratio For BER	11.2	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	7.81	-
Single Bit Pulse Width, Tb, ns	147.6	-
Channel Response Time, Tc, ns	-	146.7
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.69
Margin for Edge Jitter, EMI, other, dB	7.1	-

Table 10. Receiver Data and Calculated Performance for Standard Operation at 1.152 Mbit/s

B.4.5. 1.152 Mbit/s Low Power Option Implementation Example

(Low power transmitter to low power receiver for 1.152 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Signal Pulse Rate, Mbit/s	1.1508	1.1532
Minimum Link Distance Upper Limit, m	0.20	
Detector Responsivity, µA/(mW/cm^2)	17.2	
Minimum Irradiance In Angular Range, µW/cm^2	22.5	
Min. Eff. Receiver Signal Detected Current, nA	386.2	-
Sunlight In-Band Photocurrent, A	8.41E-06	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.0151	
Receiver Upper 3 dB Bandwidth Limit, MHz		2.48
Receiver Input Noise Current, A	2.42E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	1.54E-12	-
Sunlight Ambient Noise Current, A	3.23E-09	-
Total Receiver Input rms Noise Current, A	4.03E-09	-
Comparator Threshold = 0.5(Signal), nA	193.1	-
Receiver Signal Detected/Input Noise Current	95.8	-
Specified Signal/Noise Ratio For BER	11.2	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	9.32	-
Single Bit Pulse Width, Tb, ns	147.6	-
Channel Response Time, Tc, ns	-	146.7
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.69
Margin for Edge Jitter, EMI, other, dB	8.6	-

Table 11. Receiver Data and Calculated Performance for Low Power Operation at 1.152 Mbit/s

B.4.6. 1.152 Mbit/s Lower Power/Standard Implementation Example

(Low power transmitter to standard receiver for 1.152 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Signal Pulse Rate, Mbit/s	1.1508	1.1532
Minimum Link Distance Upper Limit, m	0.30	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	10	
Min. Eff. Receiver Signal Detected Current, nA	439.4	-
Sunlight In-Band Photocurrent, A	2.15E-05	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.0151	
Receiver Upper 3 dB Bandwidth Limit, MHz		2.48
Receiver Input Noise Current, A	3.92E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	2.50E-12	-
Sunlight Ambient Noise Current, A	5.17E-09	-
Total Receiver Input rms Noise Current, A	6.49E-09	-
Comparator Threshold = 0.5(Signal), nA	219.7	-
Receiver Signal Detected/Input Noise Current	67.8	-
Specified Signal/Noise Ratio For BER	11.2	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	7.81	-
Single Bit Pulse Width, Tb, ns	147.6	-
Channel Response Time, Tc, ns	-	146.7
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.69
Margin for Edge Jitter, EMI, other, dB	7.1	-

Table 12. Receiver Data and Calculated Performance for Standard Receiver & Low Power Transmitter Operation at 1.152 Mbit/s

B.4.7. 4.0 Mbit/s Standard Implementation Example

(Standard transmitter to standard receiver for 4.0 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Chip Rate, Mbit/s	7.9992	8.0008
Minimum Link Distance Upper Limit, m	1.0	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	10.0	
Min. Eff. Receiver Signal Detected Current, nA	439.4	-
Sunlight In-Band Photocurrent, A	2.15E-05	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.040	
Receiver Upper 3 dB Bandwidth Limit, MHz		6.04
Receiver Input Noise Current, A	4.87E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	1.99E-12	-
Sunlight Ambient Noise Current, A	8.06E-09	-
Total Receiver Input rms Noise Current, A	9.42E-09	-
Comparator Threshold = 0.5(Signal), nA	219.7	-
Receiver Signal Detected/Input Noise Current	46.7	-
Specified Signal/Noise Ratio For BER	11.5	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	6.10	-
Single Bit Pulse Width, Tb, ns	115	-
Channel Response Time, Tc, ns	-	70.4
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.51
Margin for Edge Jitter, EMI, other, dB	5.6	-

Table 13. Receiver Data and Calculated Performance for Standard Operation at 4.0 MBIT/S

B.4.8. 4.0 Mbit/s Low Power Option Implementation Example

(Low power transmitter to low power receiver for 4.0 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Chip Rate, Mbit/s	7.9992	8.0008
Minimum Link Distance Upper Limit, m	0.20	
Detector Responsivity, µA/(mW/cm^2)	17.2	
Minimum Irradiance In Angular Range, µW/cm^2	22.5	
Min. Eff. Receiver Signal Detected Current, nA	386.2	-
Sunlight In-Band Photocurrent, A	8.41E-06	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.040	
Receiver Upper 3 dB Bandwidth Limit, MHz		6.04
Receiver Input Noise Current, A	3.00E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	1.23E-12	-
Sunlight Ambient Noise Current, A	5.04E-09	-
Total Receiver Input rms Noise Current, A	5.86E-09	-
Comparator Threshold = 0.5(Signal), nA	193.1	-
Receiver Signal Detected/Input Noise Current	65.9	-
Specified Signal/Noise Ratio For BER	11.5	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	7.60	-
Single Bit Pulse Width, Tb, ns	115	-
Channel Response Time, Tc, ns	-	70.4
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.51
Margin for Edge Jitter, EMI, other, dB	7.1	-

Table 14. Receiver Data and Calculated Performance for Low Power Operation at 4.0 Mbit/s

B.4.9. 4.0 Mbit/s Low Power/Standard Implementation Example

(Low power transmitter to standard receiver for 4.0 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Chip Rate, Mbit/s	7.9992	8.0008
Minimum Link Distance Upper Limit, m	0.30	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	10.0	
Min. Eff. Receiver Signal Detected Current, nA	439.4	-
Sunlight In-Band Photocurrent, A	2.15E-05	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.040	
Receiver Upper 3 dB Bandwidth Limit, MHz		6.04
Receiver Input Noise Current, A	4.87E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	1.99E-12	-
Sunlight Ambient Noise Current, A	8.06E-09	-
Total Receiver Input rms Noise Current, A	9.42E-09	-
Comparator Threshold = 0.5(Signal), nA	219.7	-
Receiver Signal Detected/Input Noise Current	46.7	-
Specified Signal/Noise Ratio For BER	11.5	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	6.10	-
Single Bit Pulse Width, Tb, ns	115	-
Channel Response Time, Tc, ns	-	70.4
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.51
Margin for Edge Jitter, EMI, other, dB	5.6	-

Table 15. Receiver Data and Calculated Performance for Standard Receiver & Low Power Transmitter Operation at 4.0 Mbit/s

B.4.10. 16.0 Mbit/s Standard Implementation Example

(Standard transmitter to standard receiver for 16.0 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Chip Rate, Mbit/s	23.998	24.002
Minimum Link Distance Upper Limit, m	1.0	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	10.0	
Min. Eff. Receiver Signal Detected Current, nA	440	-
Sunlight In-Band Photocurrent, A	2.15E-05	-

Receiver Lower 3 dB Bandwidth Limit, MHz	0.09	0.14
Receiver Upper 3 dB Bandwidth Limit, MHz	12.0	14.5 (nominal value)
Receiver Input Noise Current, A	14.8E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	3.90E-12	-
Sunlight Ambient Noise Current, A	8.06E-09	-
Total Receiver Input rms Noise Current, A	16.85E-09	-
Comparator Threshold = 0.5(Signal), nA	228.4	-
Receiver Signal Detected/Input Noise Current	26.11	-
Specified Signal/Noise Ratio For BER	11.5	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	6.0	-
Single Bit Pulse Width, Tb, ns	38.3	45.0
Channel Response Time, Tc, ns	-	30.7
Penalty: Eye Loss for Bandwidth Limits, dB	-	2.77
Margin for Edge Jitter, EMI, other, dB	1.9	-

Table 18. Receiver Data and Calculated Performance for Standard Operation at 16.0 Mbit/s

B.4.11. 16.0 Mbit/s Low Power Option Implementation Example

(Low power transmitter to low power receiver for 16.0 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Chip Rate, Mbit/s	23.998	24.002
Minimum Link Distance Upper Limit, m	0.20	
Detector Responsivity, µA/(mW/cm^2)	17.2	
Minimum Irradiance In Angular Range, µW/cm^2	22.5	
Min. Eff. Receiver Signal Detected Current, nA	387	-
Sunlight In-Band Photocurrent, A	8.41E-06	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.09	0.14
Receiver Upper 3 dB Bandwidth Limit, MHz	12.0	14.5 (nominal value)
Receiver Input Noise Current, A	6.08E-09	-
Receiver Input Noise Current, A/(Hz)^0.5	1.6E-12	-
Sunlight Ambient Noise Current, A	6.53E-09	-
Total Receiver Input rms Noise Current, A	8.93E-09	-
Comparator Threshold = 0.5(Signal), nA	193.1	-
Receiver Signal Detected/Input Noise Current	43.3	-
Specified Signal/Noise Ratio For BER	11.5	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	5.81	-
Single Bit Pulse Width, Tb, ns	38.3	45.0
Channel Response Time, Tc, ns	-	30.7
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.77
Margin for Edge Jitter, EMI, other, dB	2.53	-

Table 19. Receiver Data and Calculated Performance for Low Power Operation at 16.0 Mbit/s

B.4.12. 16.0 Mbit/s Low Power/Standard Implementation Example

(Low power transmitter to standard receiver for 4.0 Mbit/s)

RECEIVER REQUIREMENTS & CALCULATED PERFORMANCE (Not Interface Specifications)	**Minimum**	**Maximum**
Chip Rate, Mbit/s	23.998	24.002
Minimum Link Distance Upper Limit, m	0.30	
Detector Responsivity, µA/(mW/cm^2)	44	
Minimum Irradiance In Angular Range, µW/cm^2	10.0	
Min. Eff. Receiver Signal Detected Current, nA	440	-
Sunlight In-Band Photocurrent, A	2.15E-05	-
Receiver Lower 3 dB Bandwidth Limit, MHz	0.09	0.14
Receiver Upper 3 dB Bandwidth Limit, MHz	12.0	14.5 (nominal value)
Receiver Input Noise Current, A	11.79e-9	-
Receiver Input Noise Current, A/(Hz)^0.5	3.11e-12	-
Sunlight Ambient Noise Current, A	12.48e-9	-
Total Receiver Input rms Noise Current, A	17.06e-9	-
Comparator Threshold = 0.5(Signal), nA	220	-
Receiver Signal Detected/Input Noise Current	25.75	-
Specified Signal/Noise Ratio For BER	11.5	-
Receiver Margin (Min. S/N)/(Spec. S/N), dB	3.53	-
Single Bit Pulse Width, Tb, ns	38.3	45.0
Channel Response Time, Tc, ns	-	30.7
Penalty: Eye Loss for Bandwidth Limits, dB	-	0.66
Margin for Edge Jitter, EMI, other, dB	0.25	-

Table 20. Receiver Data and Calculated Performance for Standard Receiver & Low Power Transmitter Operation at 16.0 Mbit/s

B.5. VFIR Decoder/Encoder Implementation Example

Example in this section are provided to show the VFIR decoder and encoder implemetation.

B.5.1. Reference Implementation of the HHH(1,13) Encoder

Figure 15 shows the reference implementation of the HHH(1, 13) encoder specified by the equations in Section 5.5.2. The purpose of this figure and Table 21 is to illustrate how on the time scale the encoder's data inputs (d1, d2) are related to the encoder's output triplets (Y1, Y2, Y3); each of these output triplets, also called codewords, carries the information of a specific pair of input bits. Note that, throughout this document, increasing indexes in the signal vectors mean increasing time in the respective serial signal streams. Correct interpretation and implementation of the HHH(1, 13) code requires that a pair of specific input bits D = (d1, d2) ≡ (δ1, δ2) arriving at the encoder's input in the time interval nT (1/T = 24 MHz is the chip frequency) must first be "absorbed" into the next state N ≡

($\eta1$, $\eta2$, $\eta3$) and then into the state S ≡ ($\sigma1$, $\sigma2$, $\sigma3$) before the internal codeword C ≡ ($\gamma1$, $\gamma2$, $\gamma3$) associated with ($\delta1$, $\delta2$) can be computed. In Fig. 15, the next state N ≡ ($\eta1$, $\eta2$, $\eta3$) associated with the data bits ($\delta1$, $\delta2$) occurs in the time interval (n+9)T, i.e, three encoding cycles (one encoding cycle has duration 3T) after the data bits ($\delta1$, $\delta2$) have arrived at the encoder input. In the next cycle, (n+12)T, S ≡ ($\sigma1$, $\sigma2$, $\sigma3$) takes on the value of N and the inner codeword C ≡ ($\gamma1$, $\gamma2$, $\gamma3$) now associated with ($\delta1$, $\delta2$) is being computed; it takes one further encoding cycle before this codeword C becomes available as the encoder's output codeword Y ≡ ($\delta1$, $\delta2$, $\delta3$) associated with ($\delta1$, $\delta2$). The encoding process yields therefore a delay of five encoding cycles or, equivalently, of 5×3T = 15T seconds.

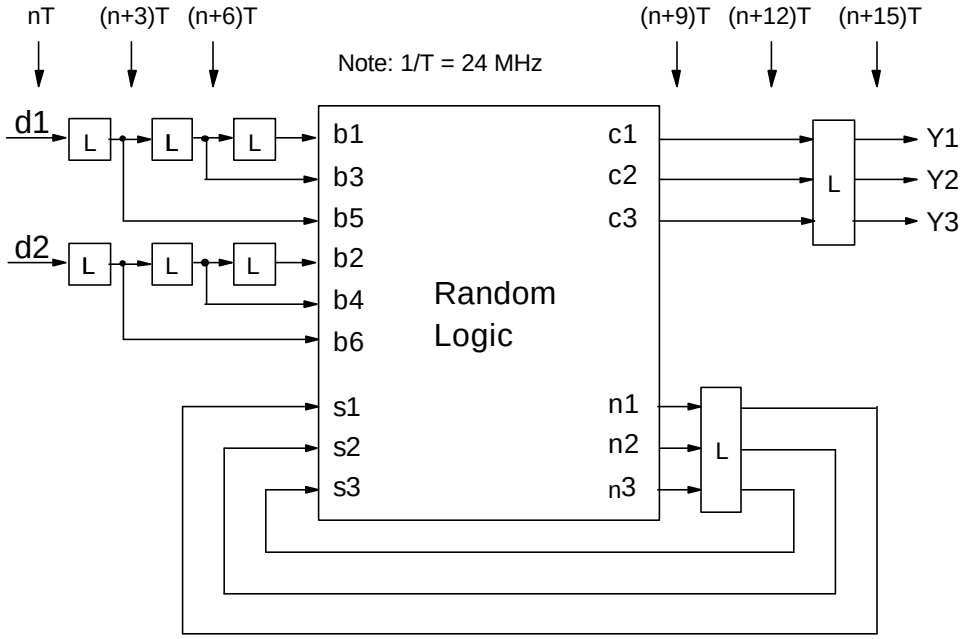


Fig. 15: The reference implementation of the HHH(1, 13) encoder indicating the inherent pipelining of codeword generation. The equations for the random logic that computes the next state N = (n1, n2, n3) and the inner codeword C = (c1, c2, c3), respectively, are defined in Section 5.5.2. Note that the delay of HHH(1, 13) encoding is five encoding cycles or, equivalently, 15 chips each of length T = 41.7 ns (see also Table 21).

Time Interval	…	nT	(n+3)T	(n+6)T	(n+9)T	(n+12)T	(n+15)T	…
D = (d1, d2)	…	**(d1, d2)**	(x , x)	(x , x)	(x , x)	(x , x)	(x , x)	…
N = (n1, n2, n3)	…	(x, x, x)	(x, x, x)	(x, x, x)	**(h1, h2, h3)**	(x, x, x)	**(x, x, x)**	…
S = (s1, s2, s3)	…	(x, x, x)	(x, x, x)	(x, x, x)	(x, x, x)	**(s1, s2,**	**(x, x, x)**	…
C = (c1, c2, c3)	…	(x, x, x)	(x, x, x)	(x, x, x)	(x, x, x)	**(g1, g2, g3)**	**(x, x, x)**	…
Y = (Y1, Y2, Y3)	…	(x, x, x)	(x, x, x)	(x, x, x)	(x, x, x)	(x, x, x)	**(Y1, Y2, Y3)**	…

Table 21: Table that illustrates the delay of HHH(1, 13) encoding is five encoding cycles, or 15 chips. Referring to Fig. 15, a specific data pair D ≡ ($\delta1$, $\delta2$) arriving at the encoder input in the interval nT is first associated with the next state N ≡ ($\eta1$, $\eta2$, $\eta3$) during time interval (n+9)T, when (b1, b2) ≡ ($\delta1$, $\delta2$). During the next time interval, (n+12)T, the state S takes on the value of N and – based on this state – the inner codeword C ≡ ($\gamma1$, $\gamma2$, $\gamma3$) is computed which now carries the information of ($\delta1$, $\delta2$). In the time interval (n+15)T, the encoder output associated with the data pair ($\delta1$, $\delta2$), Y ≡

(Ψ1, Ψ2, Ψ3), leaves the encoder (Note: 1/T = 24 MHz is the chip frequency and 'x' signifies *don't care*).

B.5.2. Gate-Level Implementation of the HHH(1,13) Encoder

Figure 16 shows the basic recommended gate-level implementation of the HHH(1, 13) encoder as specified by the equations in Section 5.5.2. The required initialization circuits for the state S = (s1, s2, s3) are not shown.

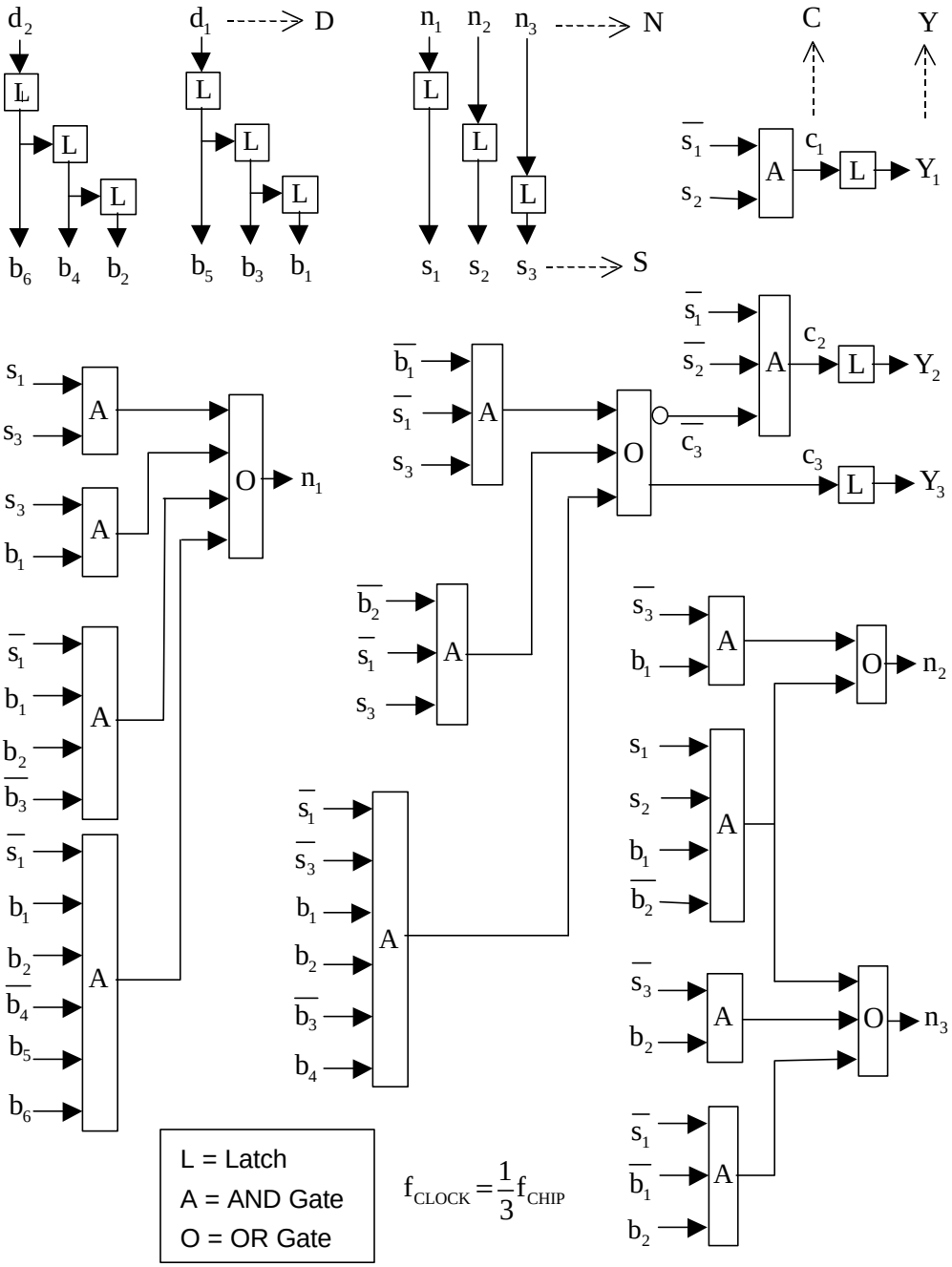


Fig. 16 Basic recommended gate-level implementation of the HHH(1, 13) encoder.

B.5.3. HHH(1,13) Decoding Equations

Define the following decoder signal vectors where increasing indexes mean increasing time in the equivalent serial signal streams:

Received codeword: $R = (r_1, r_2, r_3)$

Internal codewords:

$$Y^4 = (y_{10}, y_{11}, y_{12})$$
$$Y^3 = (y_7, y_8, y_9)$$
$$Y^2 = (y_4, y_5, y_6)$$
$$Y^1 = (y_1, y_2, y_3)$$

Internal variables:

$$Z_B = \overline{y_4 + y_5 + y_6}$$
$$Z_C = \overline{y_7 + y_8 + y_9}$$
$$Z_D = \overline{y_{10} + y_{11} + y_{12}}$$

$$X^1 = (X^1_1, X^1_2) = (x_1, x_2)$$
$$X^2 = (X^2_1, X^2_2) = (x_3, x_4)$$
$$X^3 = (X^3_1, X^3_2) = (x_5, x_6)$$

$$W = (w_1, w_2)$$
$$V = (v_1, v_2)$$

Decoder output: $U = (u_1, u_2)$

Initial conditions (start up): *None*

The components of X^1, X^2, and X^3 are computed with the following Boolean expressions (for the definition of the Boolean operator notation see Section 5.5.2 of this appendix):

$$x_1 = v_1$$
$$x_2 = (y_6 \overline{Z_C}) + (\overline{Z_B}\, Z_C\, \overline{Z_D}) + v_2$$
$$x_3 = (Z_B Z_C Z_D) + (\overline{Z_B}\, Z_C) + w_1 + w_2$$
$$x_4 = (Z_B Z_C \overline{Z_D}\, y_3) + [\overline{Z_B}\, Z_C (Z_D + \overline{y_6})] + w_2$$
$$x_5 = y_{10}$$
$$x_6 = Z_B Z_C Z_D$$

The vectors Y^1, Y^2, Y^3, Y^4, U, V, and W are outputs of latches; in every decoding cycle, they are updated as follows:

$$Y^1 \leftarrow Y^2 \leftarrow Y^3 \leftarrow Y^4 \leftarrow R \ ,$$

$$W \leftarrow X^3 \ , \quad V \leftarrow X^2 \ , \quad U \leftarrow X^1 \ ,$$

where U represents the decoded data bit pair. Note that both Z_B and Z_C can be directly obtained from delayed versions of Z_D (see also Figs. A3 and A4):

$$Z_B \leftarrow Z_C \leftarrow Z_D \ .$$

B.5.4. Reference Implementation of the HHH(1,13) Decoder

Figure 17 shows the reference implementation of the HHH(1, 13) decoder specified by the equations in Section B.5.3. The decoding delay of this decoder is four decoding cycles or 12T seconds where T = 41.7 ns.

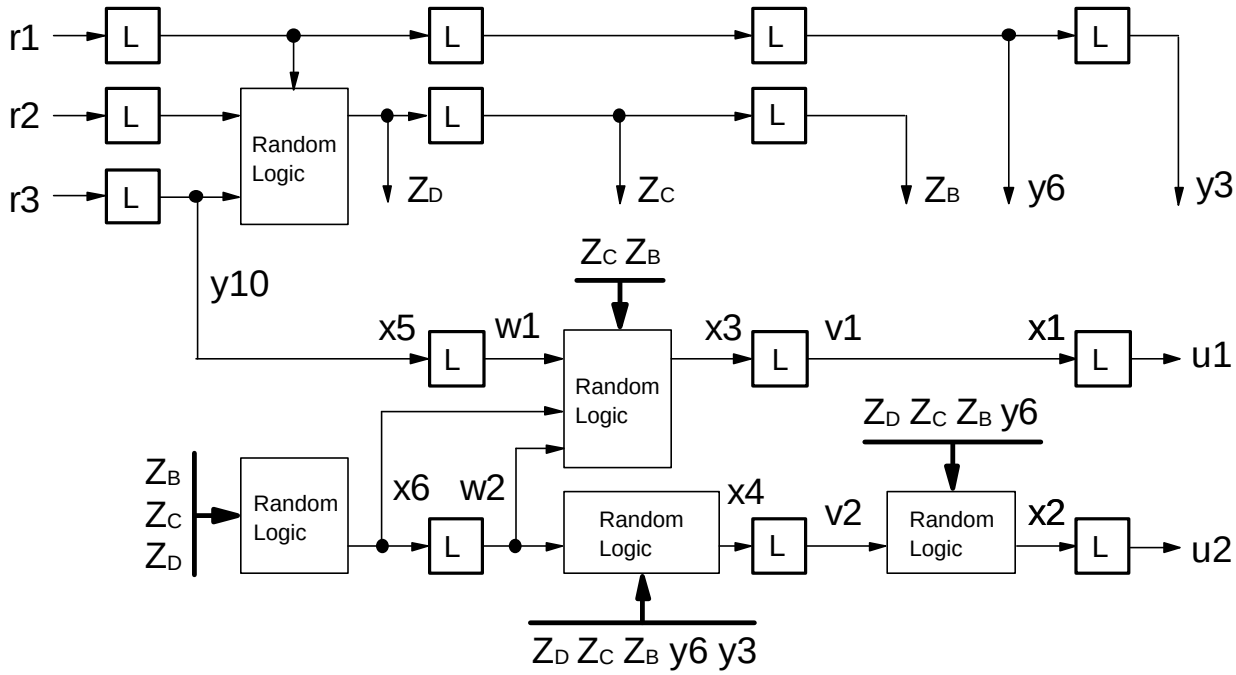
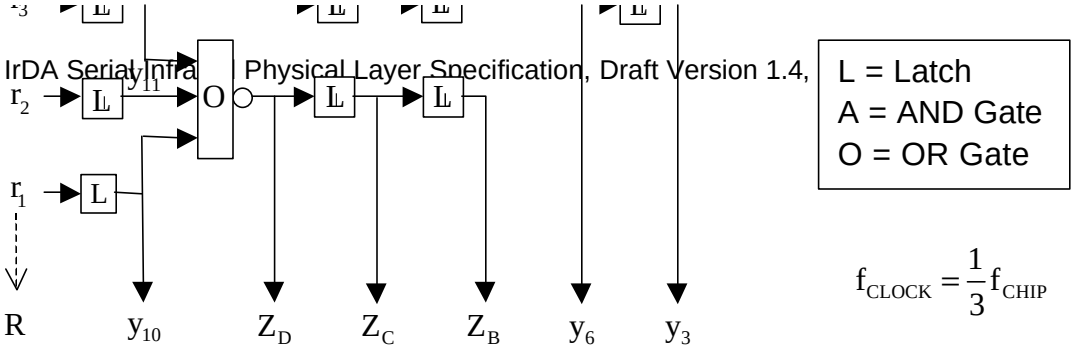


Fig. 17: The reference implementation of the HHH(1, 13) decoder. The equations for the random logic circuits that compute Z_D , x6, x4, x3, and x2, respectively, are listed in Section B.5.3 of this appendix. This form of implementation makes use of the fact that Z_B and Z_C are delayed versions of Z_D. The delay of HHH(1, 13) decoding is four decoding cycles or, equivalently, 12 chips each of length T = 41.7 ns.

B.5.5. Gate-Level Implementation of the HHH(1,13) Decoder

Figure 18. shows the basic recommended gate-level implementation of the HHH(1, 13) decoder as specified by the equations in Section B5.3. This implementation makes use of the fact that Z_B and Z_C are delayed versions of Z_D.



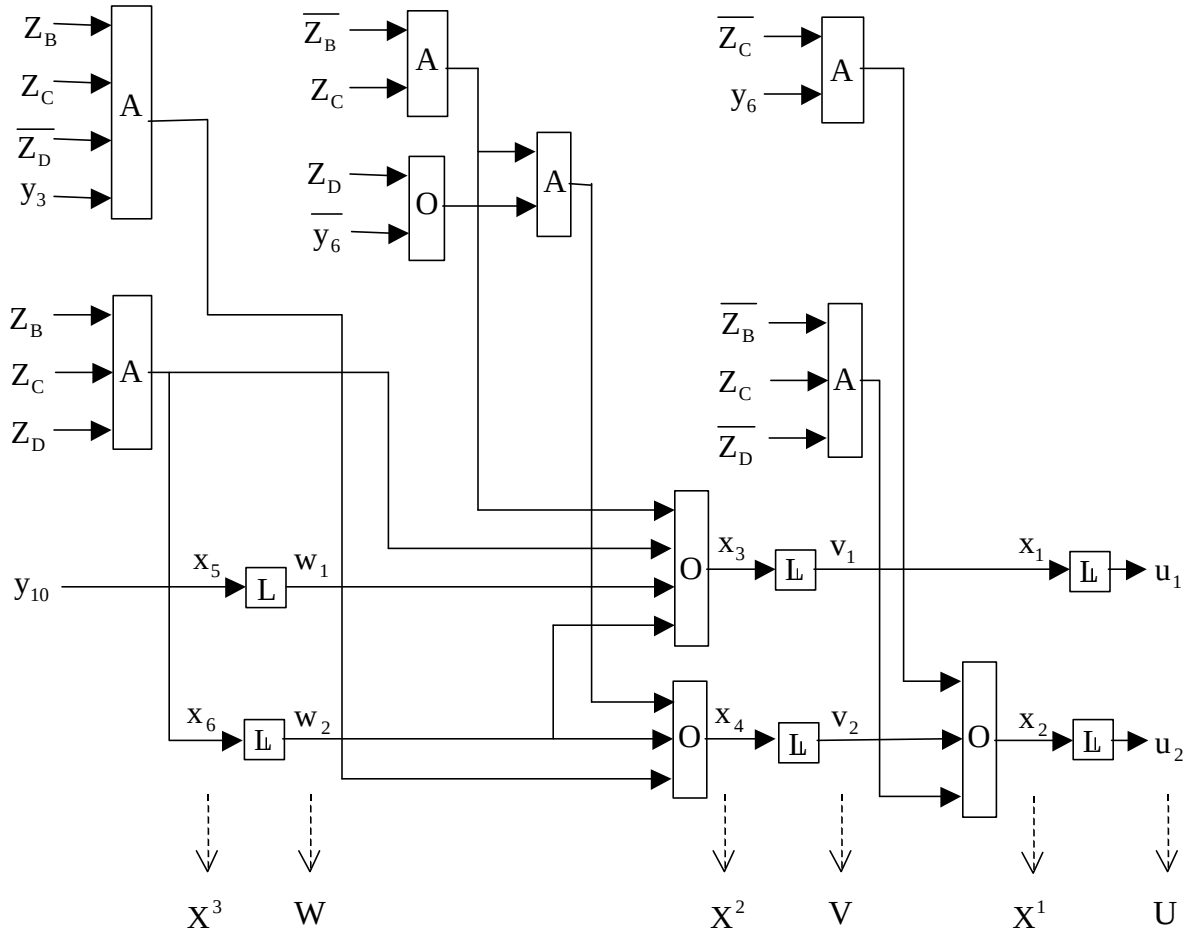


Fig. 18. Basic recommended gate-level implementation of the HHH(1, 13) decoder.

B.5.6. Encoding/Decoding Examples

EXAMPLE 1:

Scrambled payload:{(d1, d2)} = (1, 1) (0, 0) (0, 0) (0, 0) (1, 1) (0, 0) (0, 0) (0, 0)
Encoder output: {(Y1, Y2, Y3)} = (1, 0, 1) (0, 1, 0) (0, 1, 0) (0, 1, 0) (0, 0, 0) (0, 0, 0) (0, 1, 0) (0, 1, 0)
Decoded payload:{(u1, u2)} = (1, 1) (0, 0) (0, 0) (0, 0) (1, 1) (0, 0) (0, 0) (0, 0)

Legend:

a	=	time index nT, n = 0, 1, … (a = *: reset latches to logic 0)
bc	=	data input, D = (d1, d2)
d	=	control signal: d = 1 enforces N = (n1, n2, n3) = (1, 0, 0)
efghij	=	internal data, (b1, b2, b3, b4, b5, b6)
klm	=	state, S = (s1, s2, s3)
nop	=	next state, N = (n1, n2, n3)
qrs	=	internal codeword, C = (c1, c2, c3)
tuv	=	encoder output, Y = (Y1, Y2, Y3)
wx	=	data bits carried by Y
y	=	control signal: y = 1 signals valid encoder output Y
z	=	count of encoding cycles

a	bc	d	efghij	klm	nop	qrs	tuv	wx	y	z	–	**Notes:**
*	00	1	000000	000	100	010	000	00	0	*	–	Reset state / set N = (1, 0, 0)
0	**11**	1	000000	100	100	000	010	00	0	0	–	First data at input, (d1, d2) ≡ (α, β) = (1, 1)
3	**00**	1	000011	100	100	000	000	00	0	1		
6	**00**	1	001100	100	100	000	000	00	0	2		
9	**00**	0	**11**0000	**100**	011	000	000	00	0	3	–	**S = (1, 0, 0) when (b1, b2) • (a, b) = (1, 1)**
12	**11**	0	000000	011	000	101	000	00	0	4		
15	**00**	0	000011	000	000	010	**101**	11	1	5	-	First valid output Y / carries (α, β) = (1, 1)
18	**00**	0	001100	000	000	010	**010**	00	1	6		
21	**00**	0	110000	000	111	010	**010**	00	1	7	-	Last data at input, (d1, d2) = (0, 0)
24	00	0	000000	111	100	000	**010**	00	1	8	–	First flush bits at input
27	00	0	000000	100	000	000	**000**	11	1	9		
30	00	0	000000	000	000	010	**000**	00	1	10		
33	00	0	000000	000	000	010	**010**	00	1	11	-	Last flush bits at input
36	[00]	0	000000	000	000	010	**010**	00	1	12	–	Last output Y carrying data
39	[00]	0	000000	000	000	010	010	00	1	13	–	First output Y carrying flush bits
42	[00]	0	000000	000	000	010	010	00	1	14		
45	[00]	0	000000	000	000	010	010	00	1	15		
48	[00]	0	000000	000	000	010	010	00	1	16	–	Last output Y carrying flush bits

Table 22: **Encoder states for payload sequence of Example 1**. After the last flush bits have appeared at the encoder's input (time index 33), all-0 dummy data [00] is fed to the encoder during the last five encoding cycles, until the output Y carrying the last pair of flush bits becomes available (time index 48).

Legend:

a = time index nT, n = 0, 1, … (a = *: reset latches to logic 0)
bcd = received codeword, R = (r1, r2, r3)
efg = internal codeword, Y^4 = (y10, y11, y12)
hij = internal variables, (Z_D, Z_C, Z_B), where Z_C and Z_B are outputs of latches as shown in Fig. 18
kl = internal variables, W =(w1, w2)
mn = internal variables, V = (v1, v2)
op = decoder output, U = (u1, u2)
q = control signal: q = 1 signals valid decoder output
r = count of decoding cycles

a	bcd	efg	hij	kl	mn	op	q	r	–	**Notes:**
*	000	000	100	00	00	00	0	*	–	Reset state (all latches logic 0)
0	**101**	000	110	00	00	00	0	0	–	First valid received input R
3	**010**	101	011	00	11	00	0	1		
6	**010**	010	001	10	00	11	0	2		
9	**010**	010	000	00	10	00	0	3		
12	**000**	010	000	00	00	**11**	1	4	–	**First valid decoded data pair U at output**
15	**000**	000	100	00	00	**00**	1	5		
18	**010**	000	110	00	00	**00**	1	6		
21	**010**	010	011	00	11	**00**	1	7	–	Last input R carrying data
24	010	010	001	00	00	**11**	1	8	–	First input R carrying flush bits
27	010	010	000	00	00	**00**	1	9		
30	010	010	000	00	00	**00**	1	10		
33	010	010	000	00	00	**00**	1	11	–	Last valid decoded data pair U at output

Table 23: Operation of the HHH(1, 13) decoder shown in Fig. 18 for the payload of Example 1.

EXAMPLE 2:

Scrambled payload: {(d1, d2)} =	(1, 1)	(0, 1)	(0, 0)	(0, 0)	(1, 1)	(0, 1)	(0, 0)	(0, 0)
Encoder output: {(Y1, Y2, Y3)} =	(1, 0, 1)	(0, 0, 1)	(0, 1, 0)	(0, 0, 1)	(0, 0, 0)	(0, 0, 0)	(0, 1, 0)	(0, 1, 0)
Decoded payload: {(u1, u2)} =	(1, 1)	(0, 1)	(0, 0)	(0, 0)	(1, 1)	(0, 1)	(0, 0)	(0, 0)

EXAMPLE 3:

Scrambled payload: {(d1, d2)} =	(0, 1)	(0, 0)	(1, 1)	(0, 0)	(0, 0)	(1, 1)	(0, 1)	(1, 0)
Encoder output: {(Y1, Y2, Y3)} =	(0, 0, 1)	(0, 1, 0)	(0, 0, 0)	(0, 0, 0)	(0, 0, 1)	(0, 0, 0)	(0, 0, 0)	(1, 0, 0)
Decoded payload: {(u1, u2)} =	(0, 1)	(0, 0)	(1, 1)	(0, 0)	(0, 0)	(1, 1)	(0, 1)	(1, 0)